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MS-7411 Ver:10

CPU:

AMD AM2+
AMD AMD Athlon 64 X2
AMD Athlon 64 FX
AMD Athlon 64
AMD Sempron CPUs

System Chipset:

AMD - RS780M (North Bridge)
AMD - SB700 (South Bridge)

On Board Chipset:

BIOS - SPI
Azalia CODEC - Realtek ALC888
LPC Super I/O -- ITE IT8718F(GX)
LAN - REALTEK 8111C
IEEE1394 - JMB381
TPM - SLB9635TT1.2
Digital Amplifier & Sound Processor D2-92613-LR

Main Memory:

DDR II * 4 (Max 4GB)

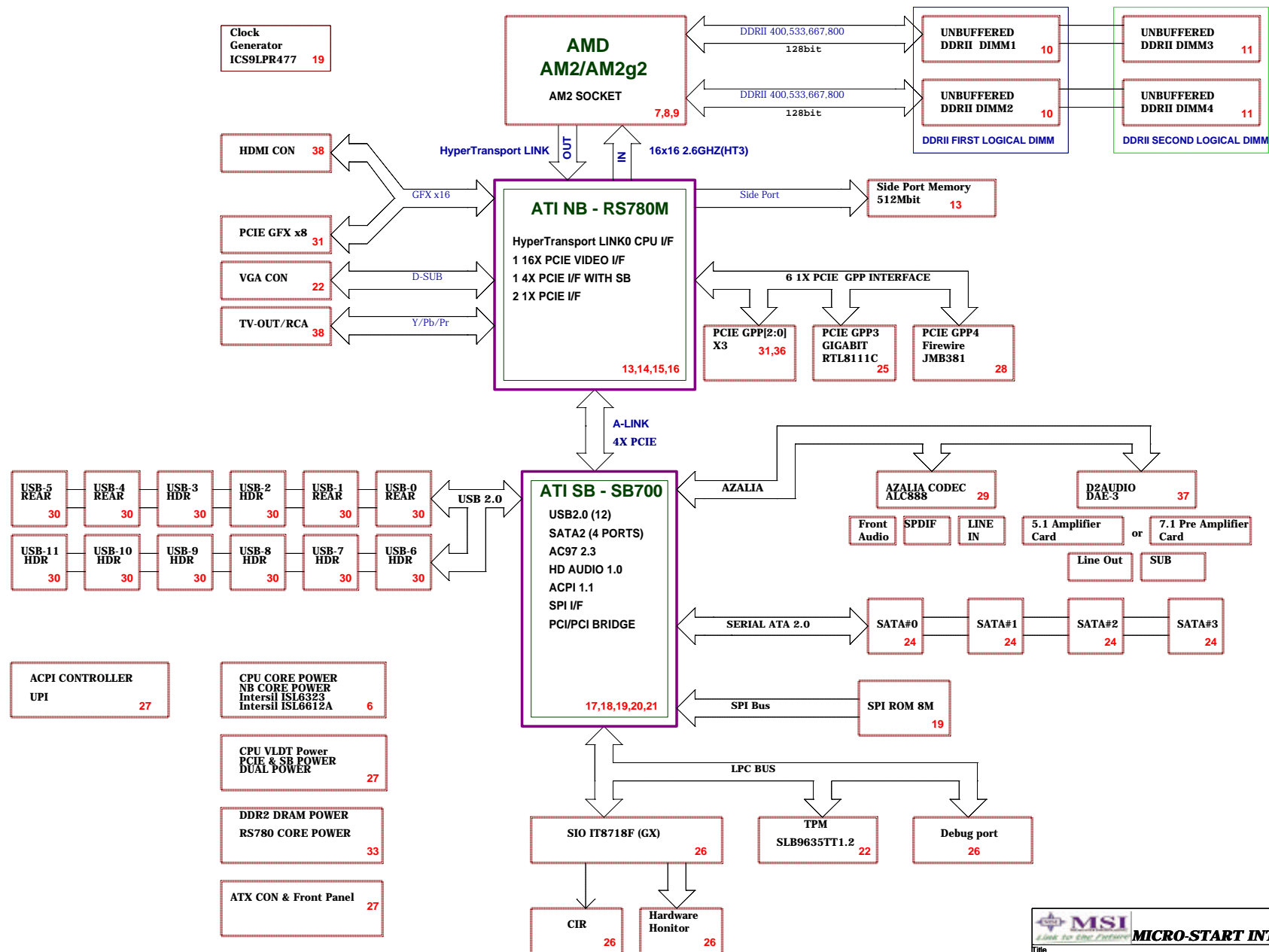
Expansion Slots:

PCI Express X16 Slot * 1
PCI Express X1 Slot * 3

Intersil PWM:

Controller - Intersil 6323 Hybrid

Project MS-7411 BLOCK DIAGRAM



SB700 GPIO Config

GPIO Name	Type	Function Description	Pin	Page
PCCLK5/GPIO41	3.3V	PCI CLK5	T3	17
REQ3#/GPIO70		REQ3#	AE6	17
REQ4#/GPIO71		REQ4#	AE6	17
GNT3#/GPIO72	Unused		AE6	17
GNT4#/GPIO73	Unused		AE5	17
INTA#/GPIO33	PCI INTA#	PCI INTA#	AD3	17
INTB#/GPIO33	PCI INTB#	PCI INTB#	AC4	17
INTC#/GPIO33	PCI INTC#	PCI INTC#	AE2	17
INTD#/GPIO33	PCI INTD#	PCI INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68	Unused		AB8	17
BMREQ/REQ5#/GPIO65	PREQ5	PREQ5	AD7	17
RIRX/EXTVNT0#	RR#	RR#	E2	18
SLP_S2/GPM9#	Unused		H7	18
GA20IN/GEVENT0#	A20GATE	A20GATE	Y15	18
KBRST#/GEVENT1#	KBRST#	KBRST#	W15	18
LPC_PME#/GEVENT3#	LPC_PME#	LPC_PME#	K4	18
LPC_SM#/EXTVNT1#	LPC_SM#	LPC_SM#	K24	18
S3_STATE/GEVENT5#	Unused		F1	18
SYS_RESET#/GPM7#	FP_RST#	FP_RST#	J2	18
WAKE#/GEVENT8#	WAKE#	WAKE#	H6	18
BLINK/GPM8#	Unused		F2	18
SMBALERT#/THRMTRIP#/GEVENT2#	SMBALERT#	SMBALERT#	J6	18
SATA_ISOP#/GPIO10	SB_GPIO10(Strapping)		AE18	18
CLK_REQ0#/SATA_IS1#/GPIO6	SB_GPIO6(Strapping)		AD18	18
SMARTVOLT/SATA_IS2#/GPIO4	SB_GPIO4(Strapping)		AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0	SB_GPIO0(Strapping)		W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39	SB_GPIO39(Strapping)		V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40	SB_GPIO40(Strapping)		W20	18
SPKR/GPIO2	SPKR	SPKR	W21	18
SCLK/GPOC0#	SCLK	SCLK	AA18	18
SDA0/GPOC1#	SDATA	SDATA	W18	18
SCLK1/GPOC2#	SCLK1	SCLK1	K1	18
SDA1/GPOC3#	SDATA1	SDATA1	K2	18
DDC1_SCL#/GPIO9	Unused		AA20	18
DDC1_SDA#/GPIO8	SPL_WP#	SPL_WP#	Y18	18
LLB#/GPIO68	LC_SENSE	LC_SENSE	C1	18
SHUTDOWN#/GPIO5	SB_GPIO5(Strapping)		Y19	18
DDR3_RST#/GEVENT7#	Unused		G5	18
USB_OC6#/IR_TX1/GEVENT5#	OC4#	OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#	OC4#	OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#	OC3#	OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#	OC3#	OC3#	A9	18
USB_OC2#/GPM2#	OC2#	OC2#	E5	18
USB_OC1#/GPM1#	OC2#	OC2#	F8	18
USB_OC0#/GPM0#	OC1#	OC1#	E4	18
AZ_SDIN0/GPIO42	SDATA_IN_R	SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43	Unused		J8	18
AZ_SDIN2/GPIO44	Unused		L8	18
AZ_SDIN3/GPIO46	Unused		M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM6#	Unused		L5	18
PS2_DAT/EC_GPIO0	Unused		H19	18
PS2_CLK/EC_GPIO1	Unused		H20	18
SPL_CS2#/EC_GPIO2	Unused		H21	18
IDE_RST#/RST#/EC_GPIO3	Unused		F25	18
PS2KB_DAT/EC_GPIO4	Unused		D22	18
PS2KB_CLK/EC_GPIO5	Unused		E24	18
PS2M_DAT/EC_GPIO6	Unused		E25	18
PS2M_CLK/EC_GPIO7	Unused		D23	18
USBCLK/14M_25M_48M_OSC	USB_48M_CLK	USB_48M_CLK	C8	18
KSD_10/EC_GPIO8	Unused		A18	18
KSD_17/EC_GPIO9	Unused		B18	18
EC_PWM0/EC_GPIO10	Unused		F21	18
SCL2/EC_GPIO11	Unused		D21	18
SDA2/EC_GPIO12	Unused		F19	18
SCL3_LV/EC_GPIO13	Unused		E20	18
SDA3_LV/EC_GPIO14	Unused		E21	18
EC_PWM1/EC_GPIO15	Unused		E19	18
EC_PWM2/EC_GPIO16	SB_GPIO16(Strapping)		D19	18
EC_PWM3/EC_GPIO17	Unused		E18	18
KSL6/EC_GPIO18	Unused		G20	18
KSL1/EC_GPIO19	Unused		G21	18
KSL2/EC_GPIO20	Unused		D25	18
KSL3/EC_GPIO21	Unused		D24	18
KSL4/EC_GPIO22	Unused		C25	18
KSL5/EC_GPIO23	Unused		C24	18
KSL6/EC_GPIO24	Unused		B25	18
KSL7/EC_GPIO25	Unused		C23	18
KSD_0/EC_GPIO26	Unused		B24	18
KSD_1/EC_GPIO27	Unused		B23	18
KSD_2/EC_GPIO28	Unused		A23	18
KSD_3/EC_GPIO29	Unused		C22	18
KSD_4/EC_GPIO30	Unused		A22	18
KSD_5/EC_GPIO31	Unused		B22	18
KSD_6/EC_GPIO32	Unused		B21	18
KSD_7/EC_GPIO33	Unused		A21	18
KSD_8/EC_GPIO34	Unused		D20	18
KSD_9/EC_GPIO35	Unused		C20	18
KSD_10/EC_GPIO36	Unused		A20	18
KSD_11/EC_GPIO37	Unused		B20	18
KSD_12/EC_GPIO38	Unused		B19	18
KSD_13/EC_GPIO39	Unused		A19	18
KSD_14/EC_GPIO40	Unused		D18	18
KSD_15/EC_GPIO41	Unused		C18	18
SATA_ACT#/GPIO67	SATA_LED#	SATA_LED#	W11	19
IDE_D0/GPIO15	Unused		AD24	19
IDE_D1/GPIO16	Unused		AD23	19
IDE_D2/GPIO17	Unused		AE22	19
IDE_D3/GPIO18	Unused		AC22	19

GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19	Unused		AD21	19
IDE_D5/GPIO20	Unused		AE20	19
IDE_D6/GPIO21	Unused		AB20	19
IDE_D7/GPIO22	Unused		AD19	19
IDE_D8/GPIO23	Unused		AE19	19
IDE_D9/GPIO24	Unused		AC20	19
IDE_D10/GPIO25	Unused		AD20	19
IDE_D11/GPIO26	Unused		AE21	19
IDE_D12/GPIO27	Unused		AB22	19
IDE_D13/GPIO28	Unused		AD22	19
IDE_D14/GPIO29	Unused		AC23	19
IDE_D15/GPIO30	Unused		AC23	19
SPL_D0/GPIO11	SPL_DATAIN	SPL_DATAIN	G6	19
SPL_D0/GPIO11	SPL_DATAOUT	SPL_DATAOUT	D2	19
SPL_CLK/GPIO47	SPL_CLK	SPL_CLK	D1	19
SPL_HOLD#/GPIO31	SPL_HOLD_L	SPL_HOLD_L	F4	19
SPL_CS#/GPIO32	SPL_CS#	SPL_CS#	F3	19
LAN_RST#/GPIO13	CPU_PRESENT#	CPU_PRESENT#	U15	19
ROM_RST#/GPIO14	Unused		J1	19
FANOUT6/GPIO3	Unused		M8	19
FANOUT1/GPIO48	COM_GPIO	COM_GPIO	M5	19
FANOUT2/GPIO49	Unused		M7	19
FANIN0/GPIO50	Unused		P5	19
FANIN1/GPIO51	Unused		P8	19
FANIN2/GPIO52	Unused		E8	19
TEMPIN0/GPIO61	Unused		B6	19
TEMPIN1/GPIO62	Unused		A6	19
TEMPIN2/GPIO63	Unused		A5	19
TEMPIN3/TALERT#/GPIO64	TALERT#	TALERT#	B5	19
VIN0/GPIO53	BIO5_WP#1	BIO5_WP#1	A4	19
VIN1/GPIO54	BIO5_WP#2	BIO5_WP#2	B4	19
VIN2/GPIO55	CLR_COM5	CLR_COM5	C4	19
VIN3/GPIO56	LAN_DISABLE	LAN_DISABLE	D4	19
VIN4/GPIO57	Unused		D5	19
VIN5/GPIO58	Unused		D6	19
VIN6/GPIO59	Unused		A7	19
VIN7/GPIO60	Unused		B7	19

Super I/O GPIO Config

GPIO Name	Type	Function Description	Pin	Page
VID05/GP27		LEO_GPIO2	20	26
VID04/GP26		LEO_GPIO1	21	26
VID01/GP21/NGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/UP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP67		MSDATA	82	26
MCLK/GP66		MSCLK	83	26
SUSC#/GP53		LPC_SM#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCRST3#/GP11		ASSID_GPIO0	34	26
PCRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26



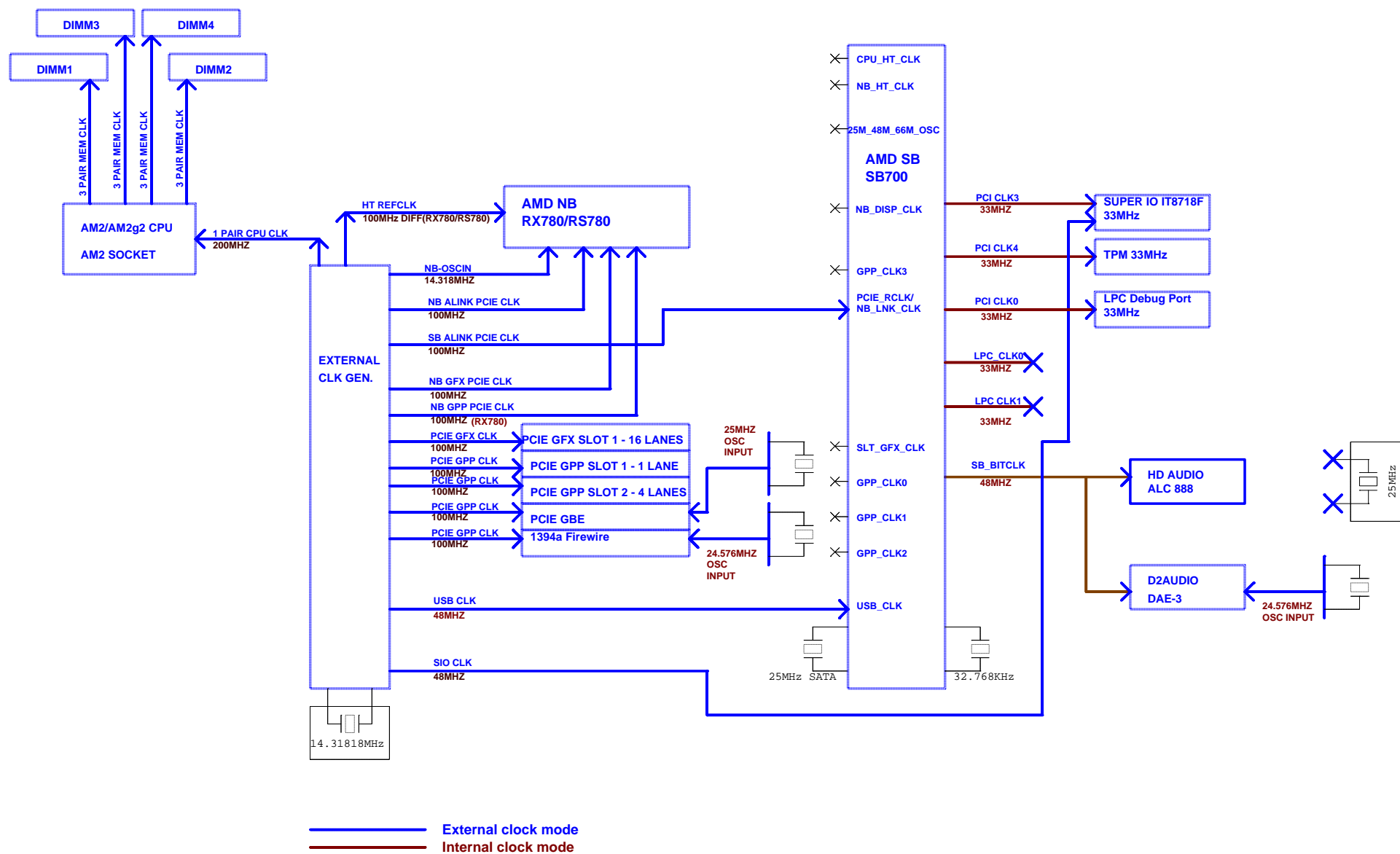
MICRO-START INTL CO.,LTD.

Title: GPIO Configuration

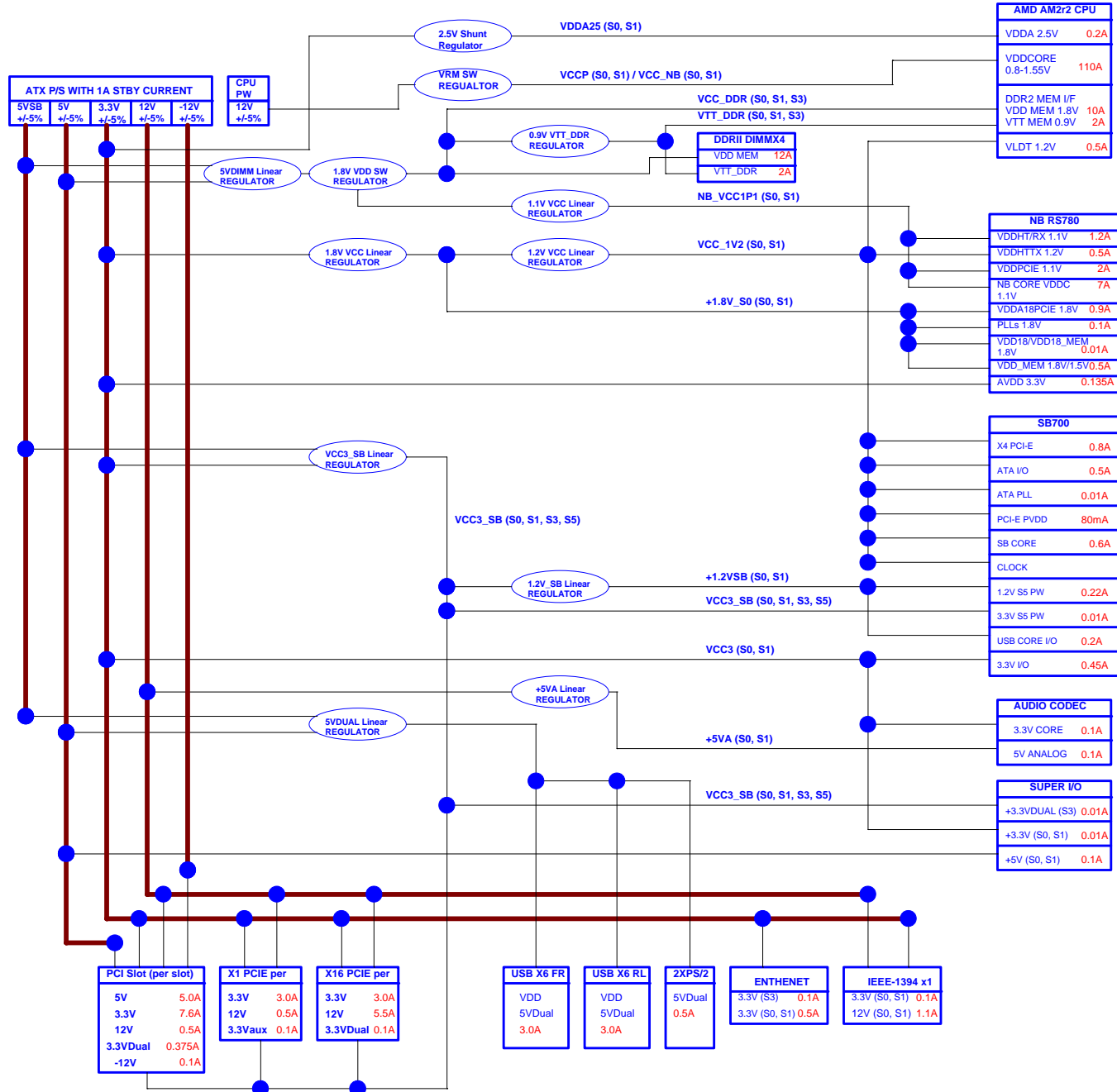
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Rev: 10

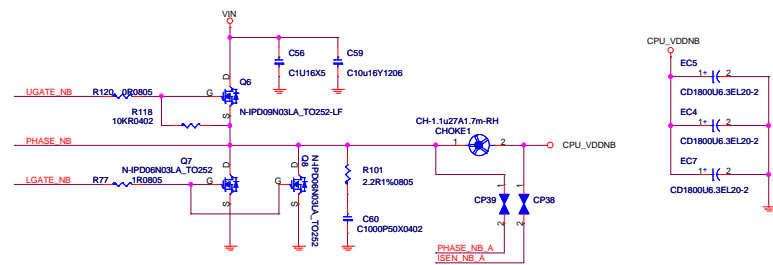
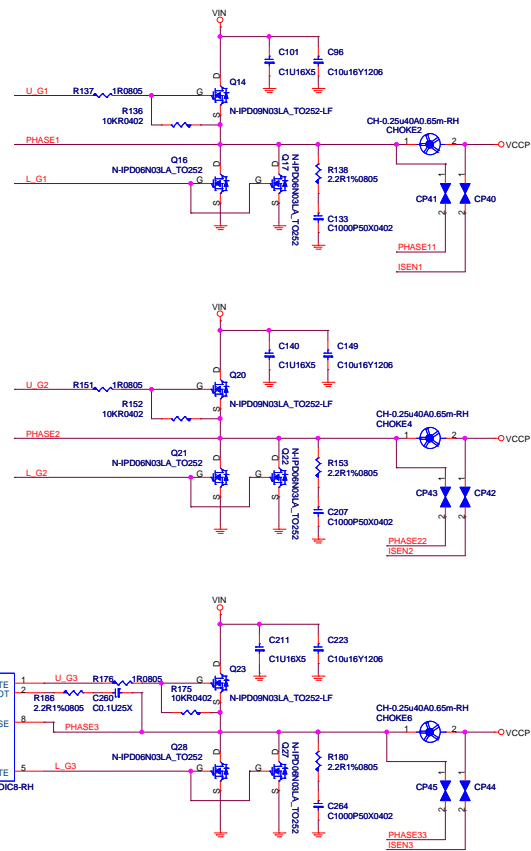
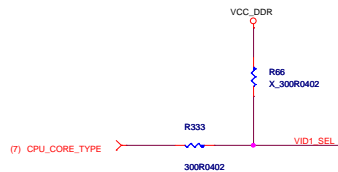
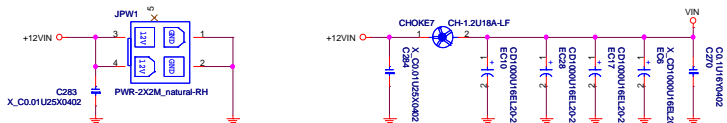
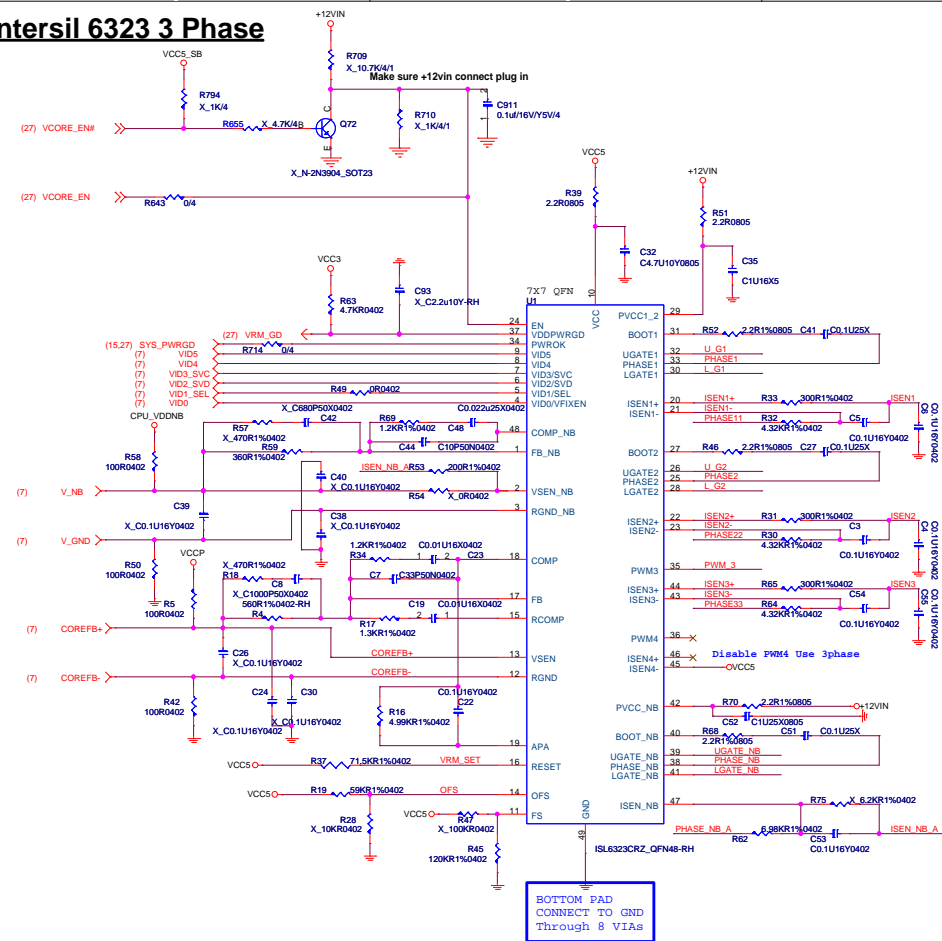
Date: Wednesday, July 23, 2008 Sheet: 3 of 40

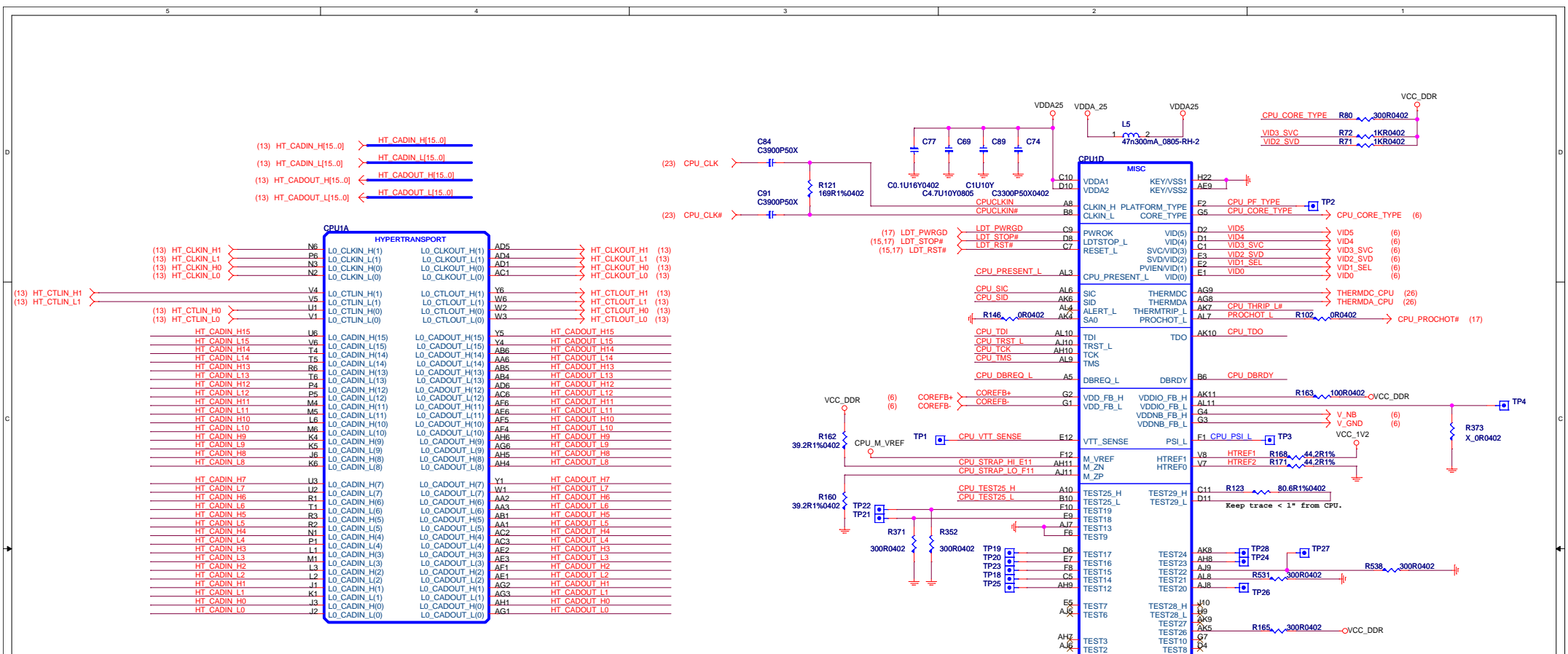


Power Deliver Chart

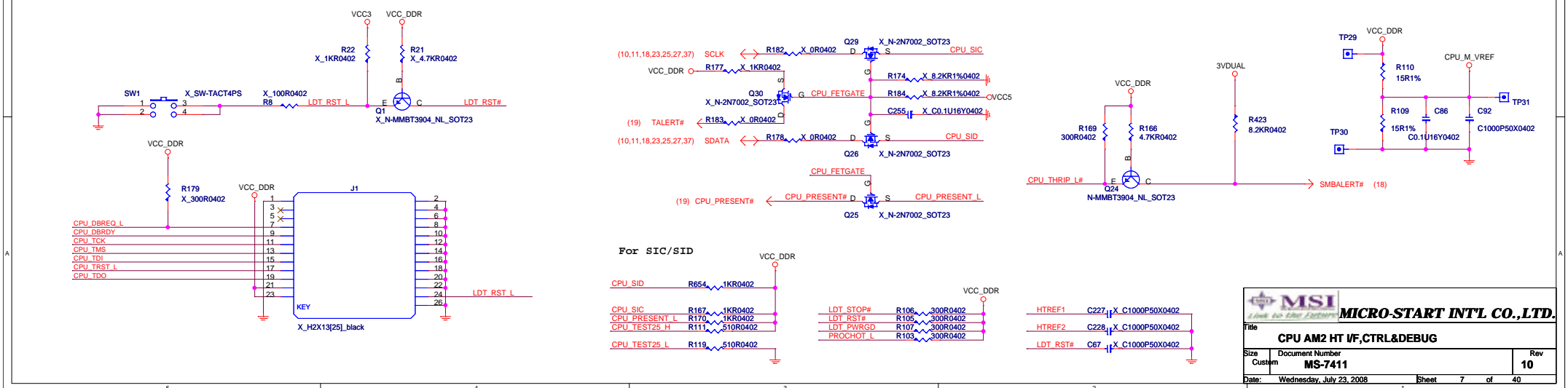


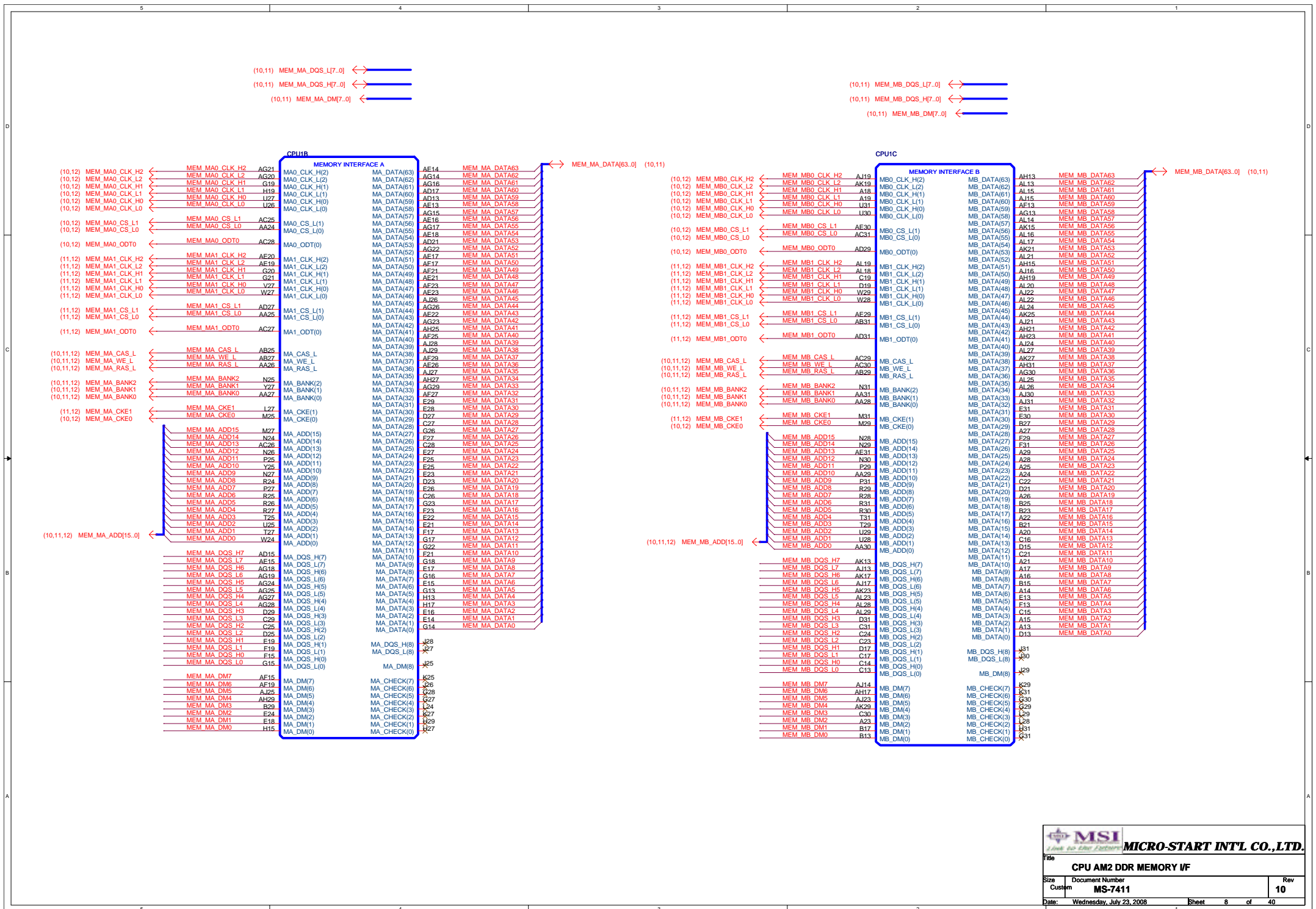
Intersil 6323 3 Phase



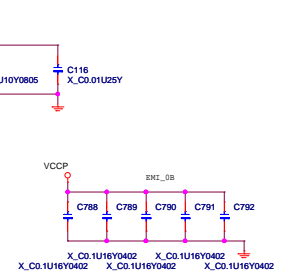
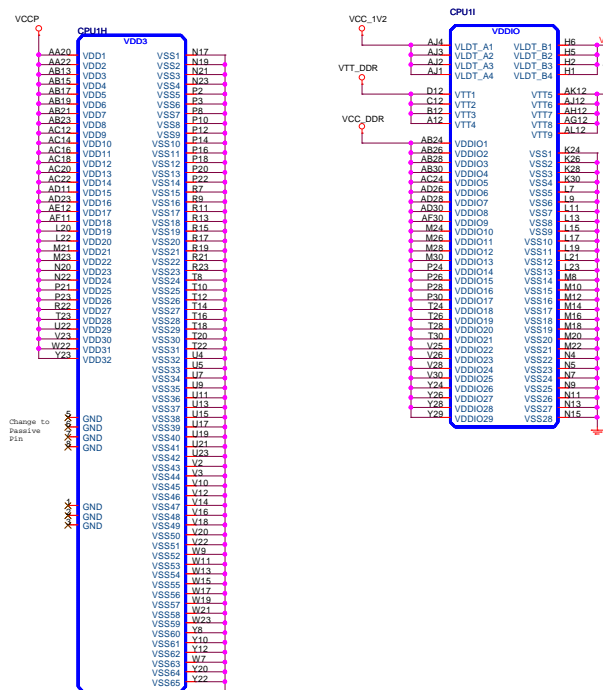
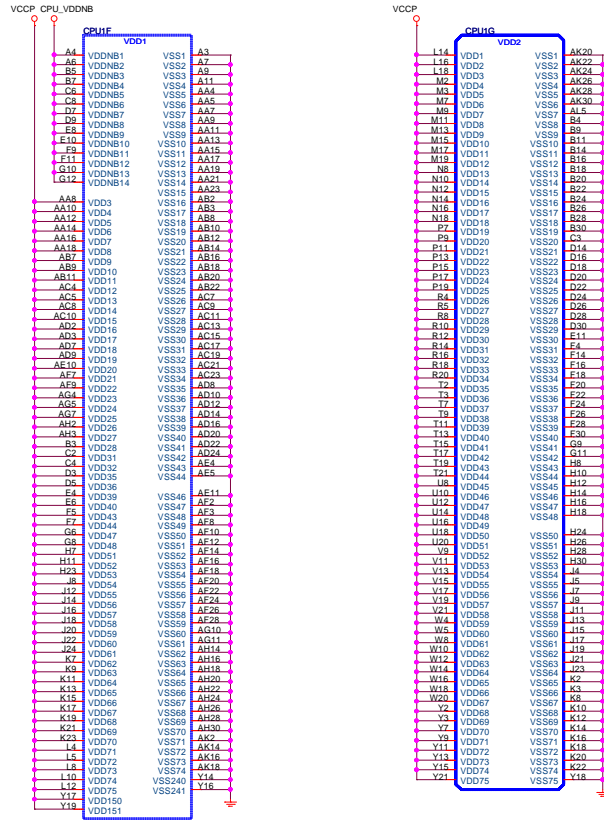


AMD REQUEST

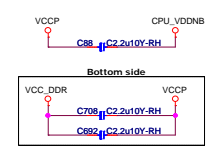
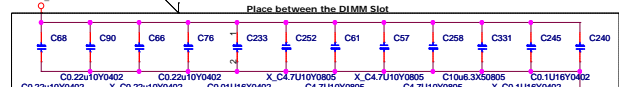
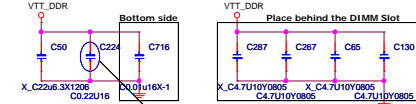
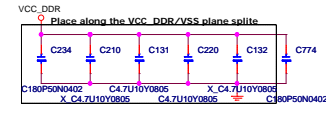
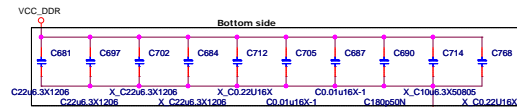
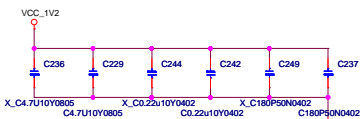
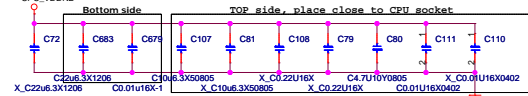
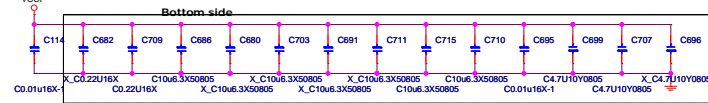
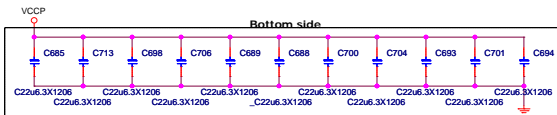


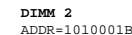
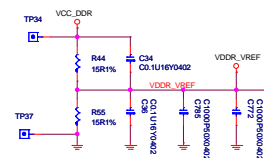


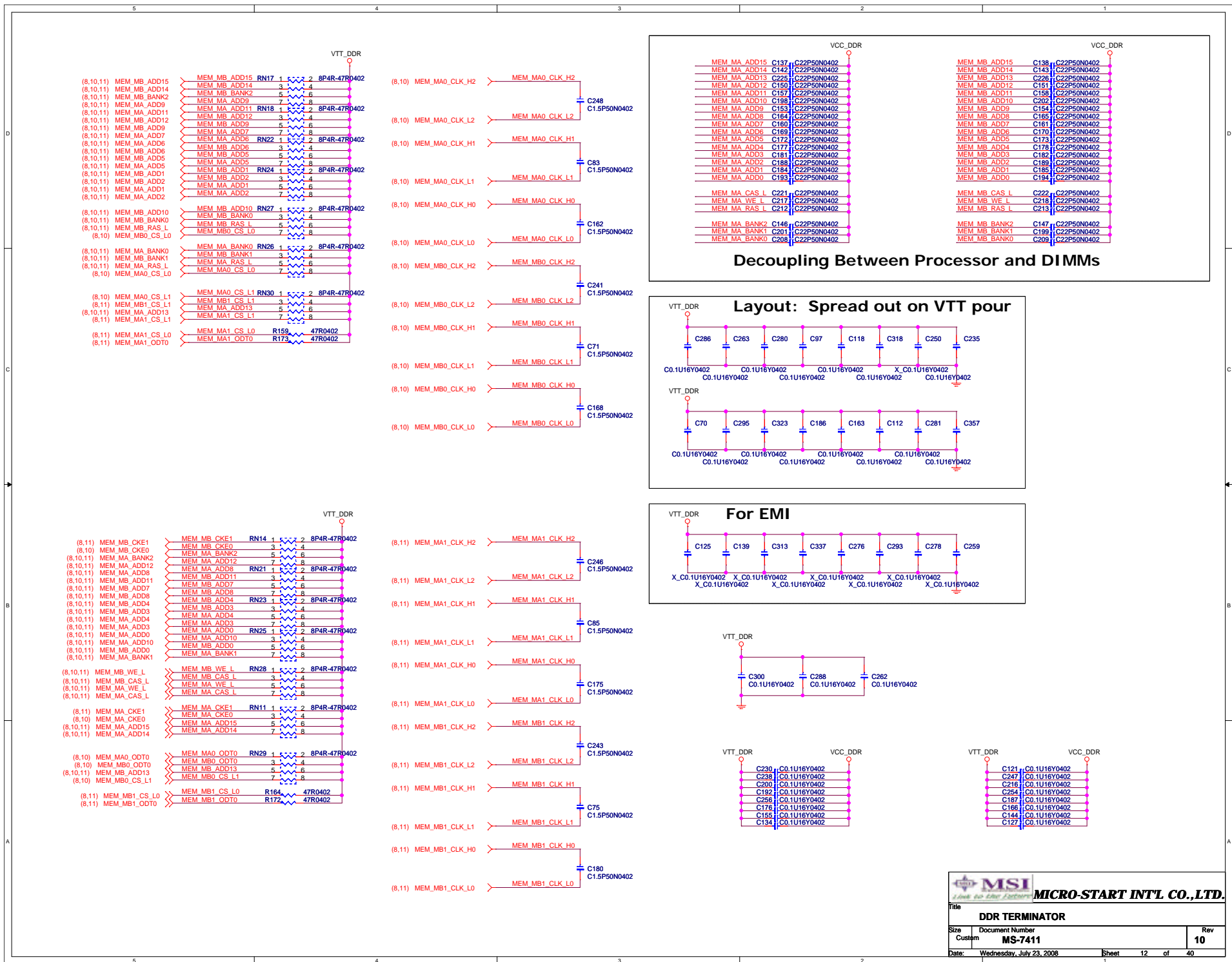
CPU AM2 PWR & GND



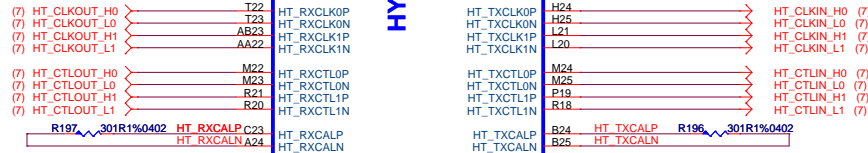
near (1900,-4700)*3, near C116*2






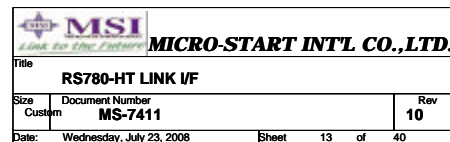


5	4	3	2	1
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2:1 minimum space:height ratio.
Place resistor(s) within 1.0" of Northbridge
balls.

VCC_1V2  VCCP
C784
X_C0.1U16Y0402



4



Stuff For RS780



	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPI00)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPI01)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPI02)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPI03)	TMD5_HPD	TMD5_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPI06)	X	AUXIN
DEBUG_OUT5	TXCLK_LP(DBG_GPI01)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPI02)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPI03)	X	AUX_CAL

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```

These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)      default:
110: 4-0-0-0-0-0    Config A
101: 4-4-0-0-0-0    Config B
100: 4-2-2-0-0-0    Config C
011: 4-2-1-1-0-0    Config D
010: 4-1-1-1-1-1    Config E
others: register defined (default to Config E)

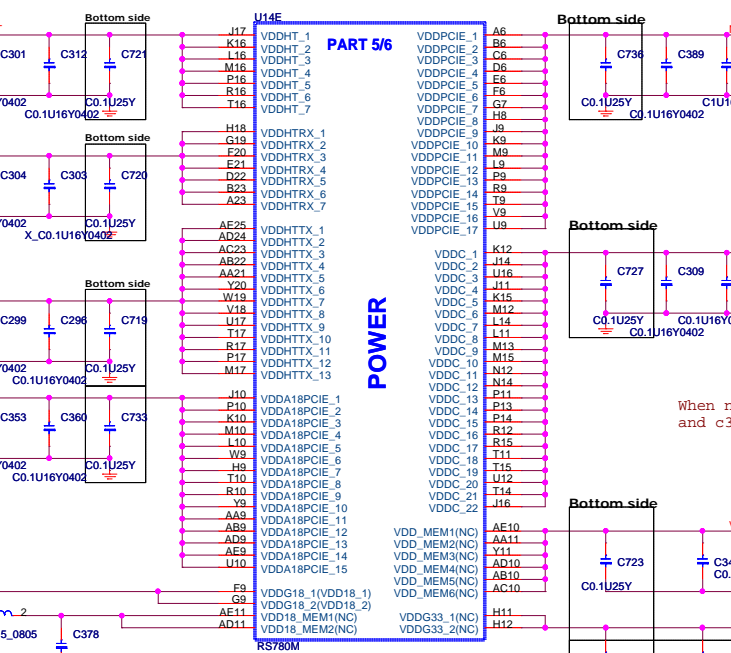
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RS740/RX780/RS780: LOAD_EEPROM_STRAPS

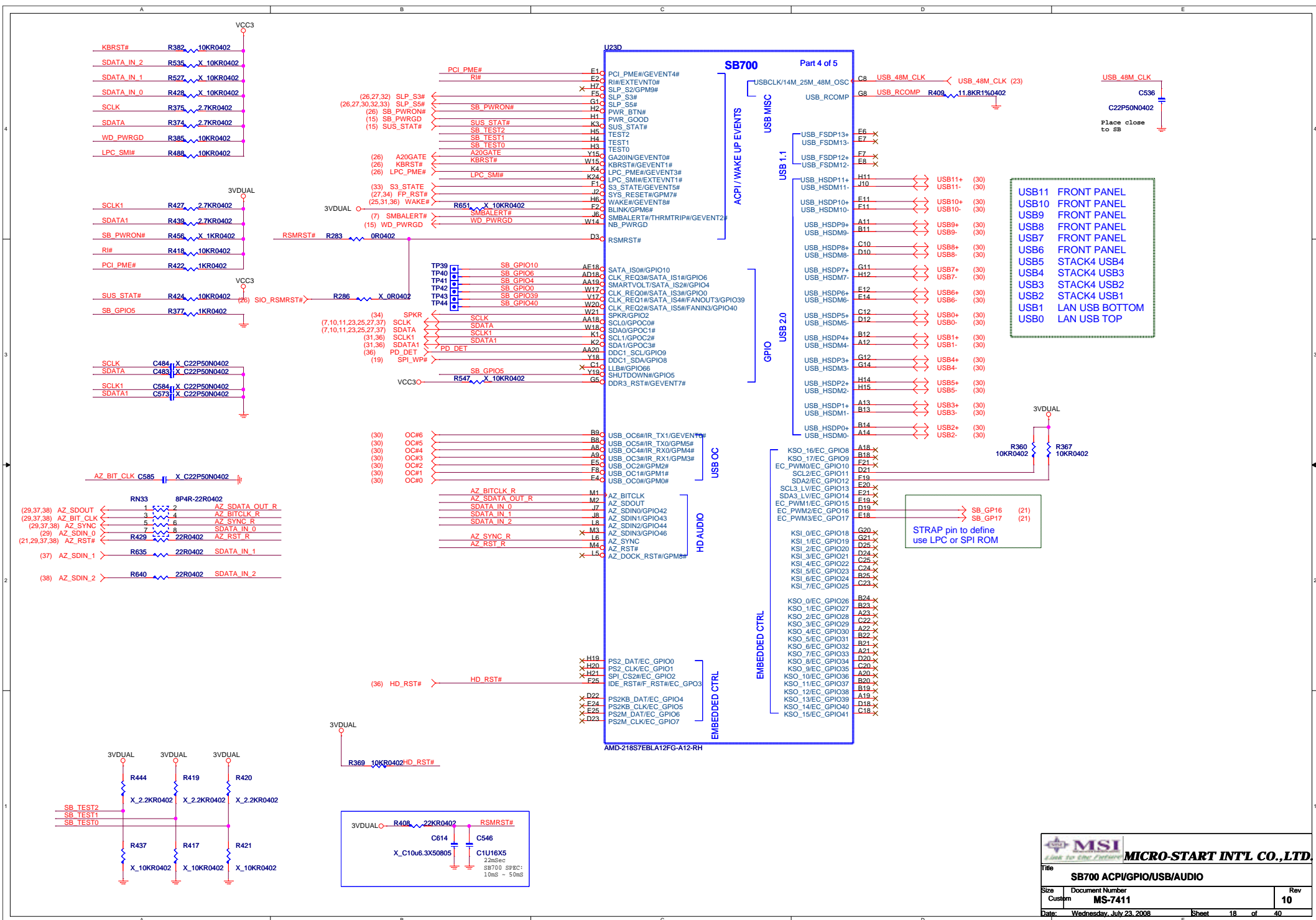
```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIOL
RX780: pin DFT_GPIOL
RS780: pin SUS_STAT#
```

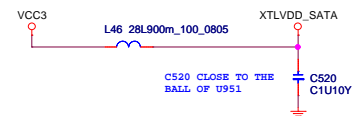
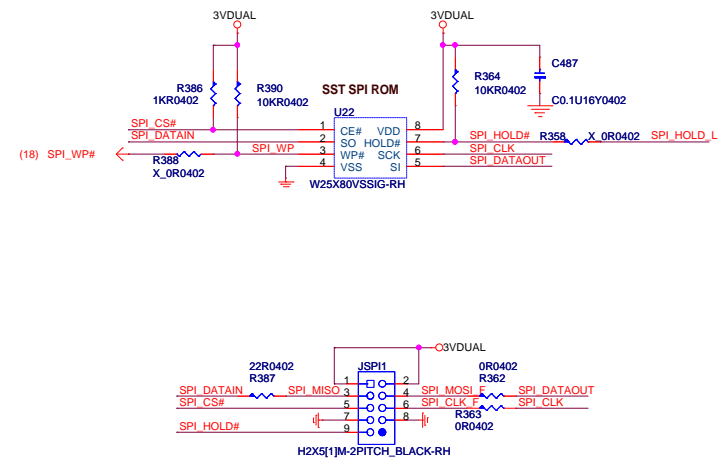
RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

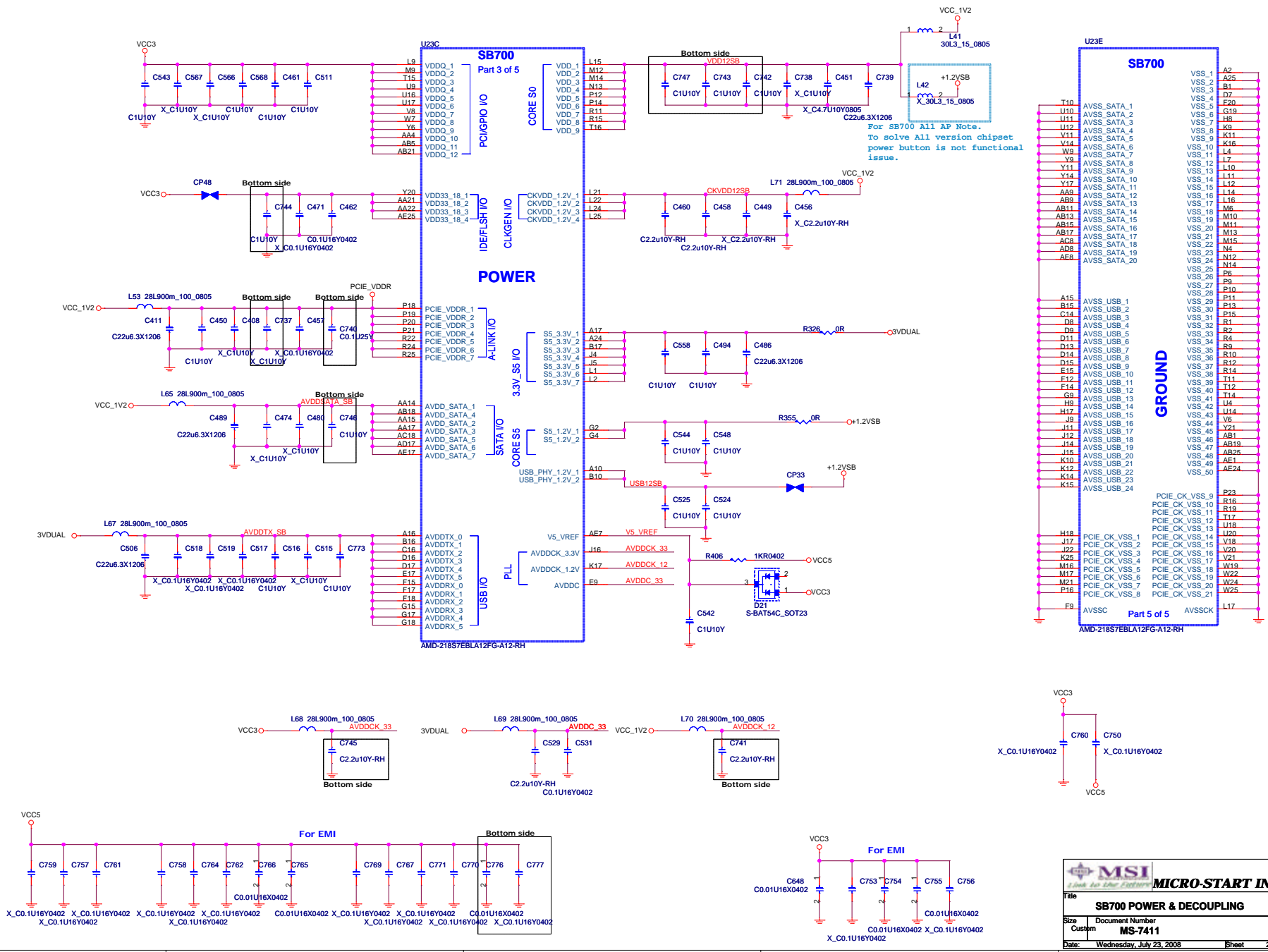
```
Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
RX780: Not Applicable
```



RS740 : 3.3V



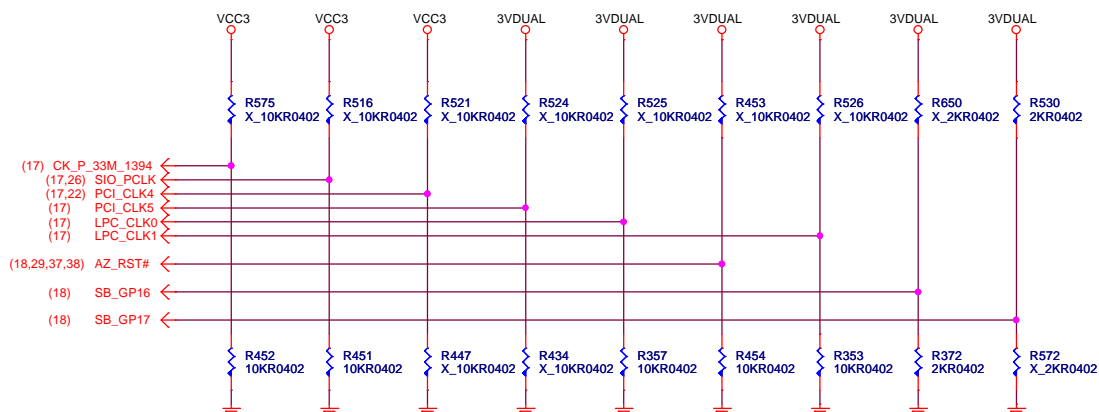






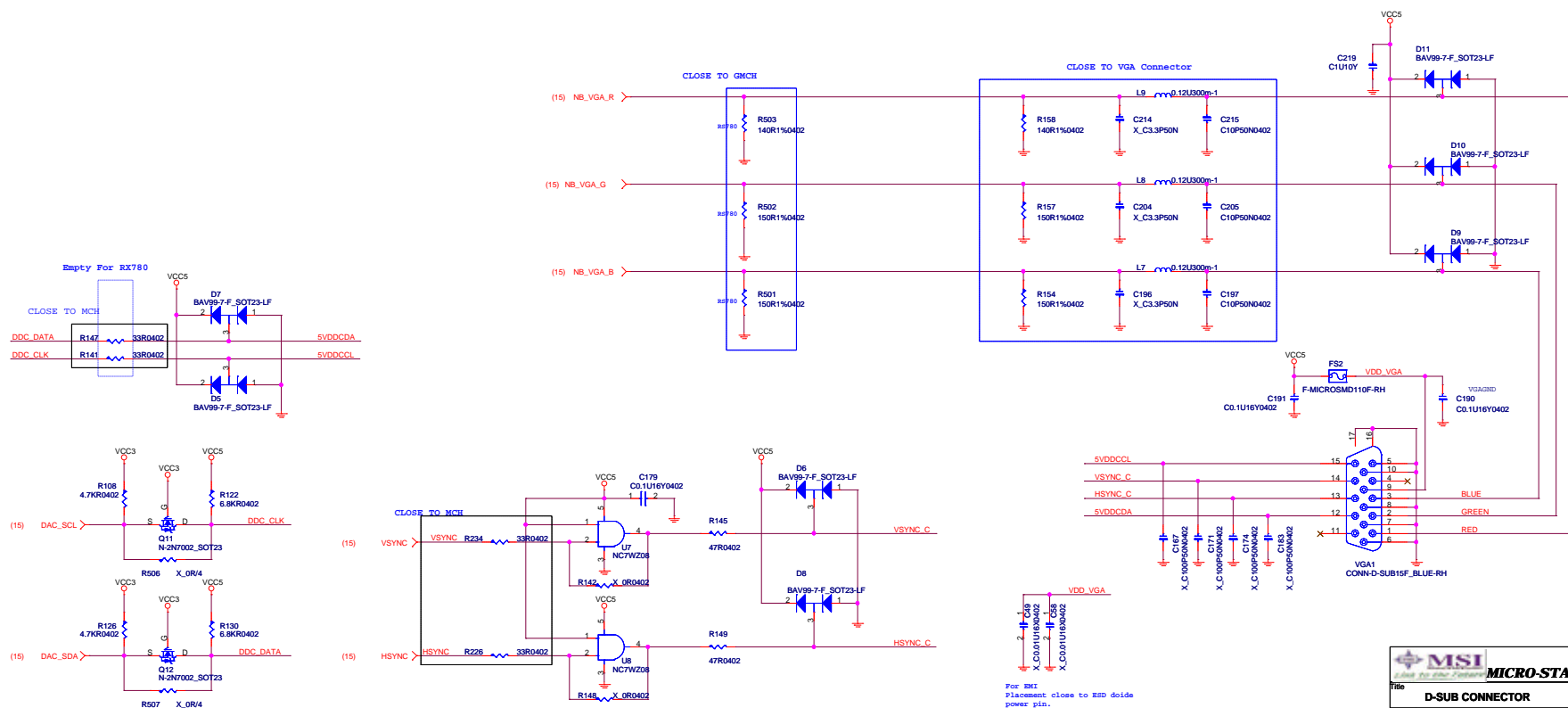
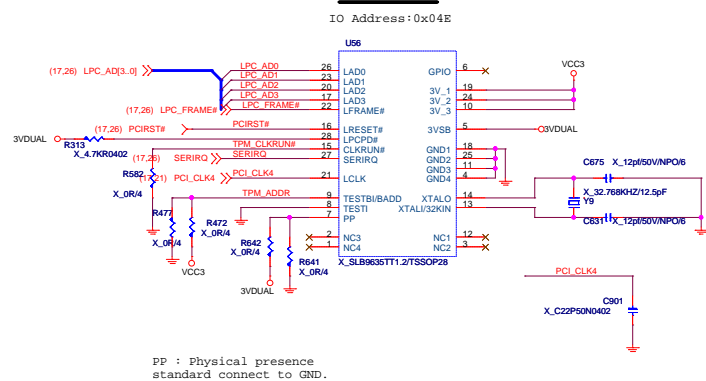
REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED

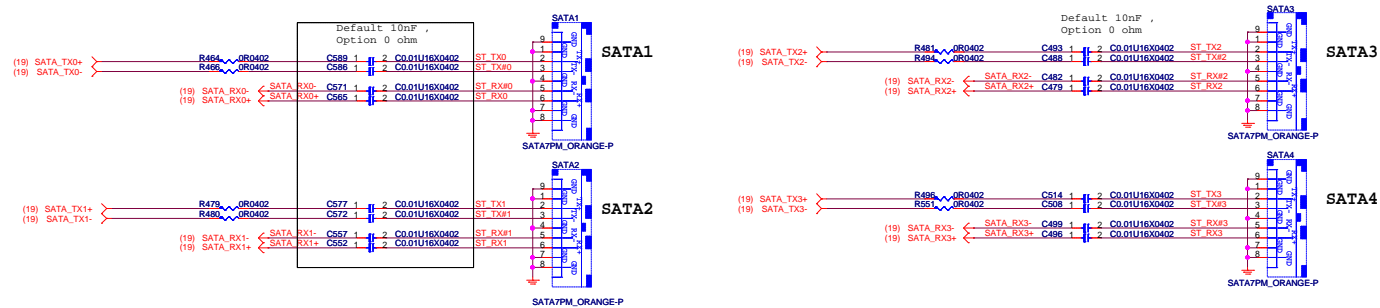


	PCI_CLK2 CK_P_33M_1394	PCI_CLK3 SIO_PCLK	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
	Watchdog timer on NB_PWGRD	Debug straps	TPM CLOCK	RESERVED	Booting from PCI Memory	Internal Clock Generator	INTERNAL RTC	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM	
PULL HIGH	ENABLED (VCC3)	ENABLED (VCC3)			ENABLED (VCC3_SB)	ENABLED (VCC3_SB)		ENABLED		
PULL LOW	DISABLED DEFAULT	DISABLED DEFAULT			DISABLED DEFAULT	DISABLED DEFAULT	NC IS EXT. RTC DEFAULT	DISABLED DEFAULT	Note: NC represents internal 10-k? 5% pull-up	

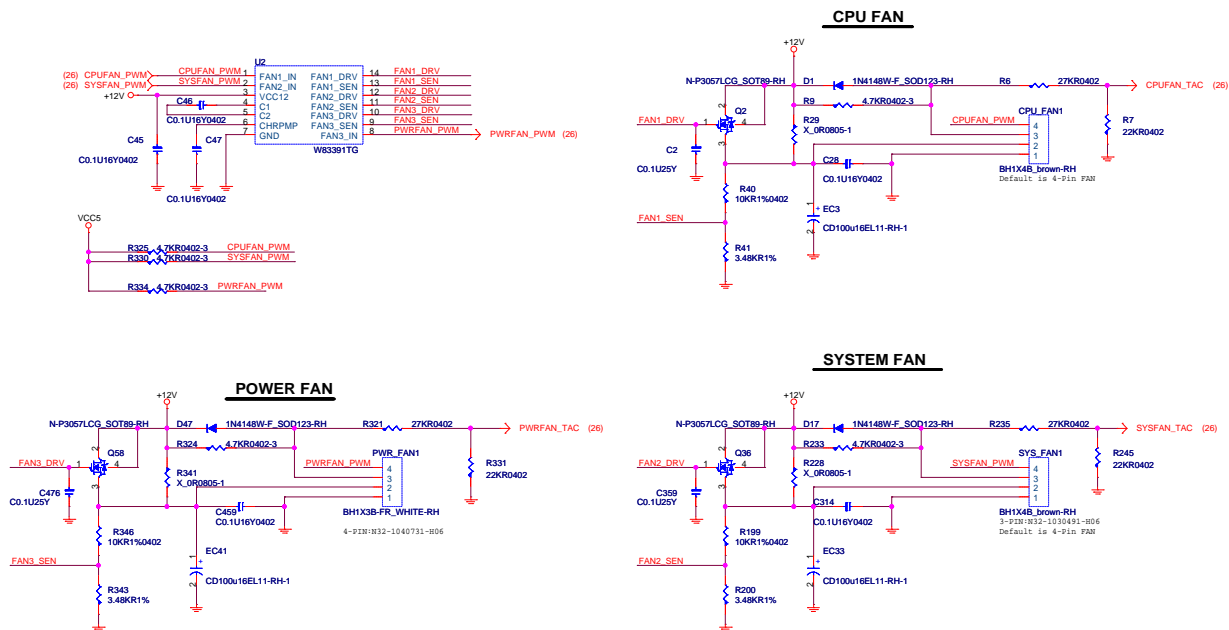
TPM Chipset



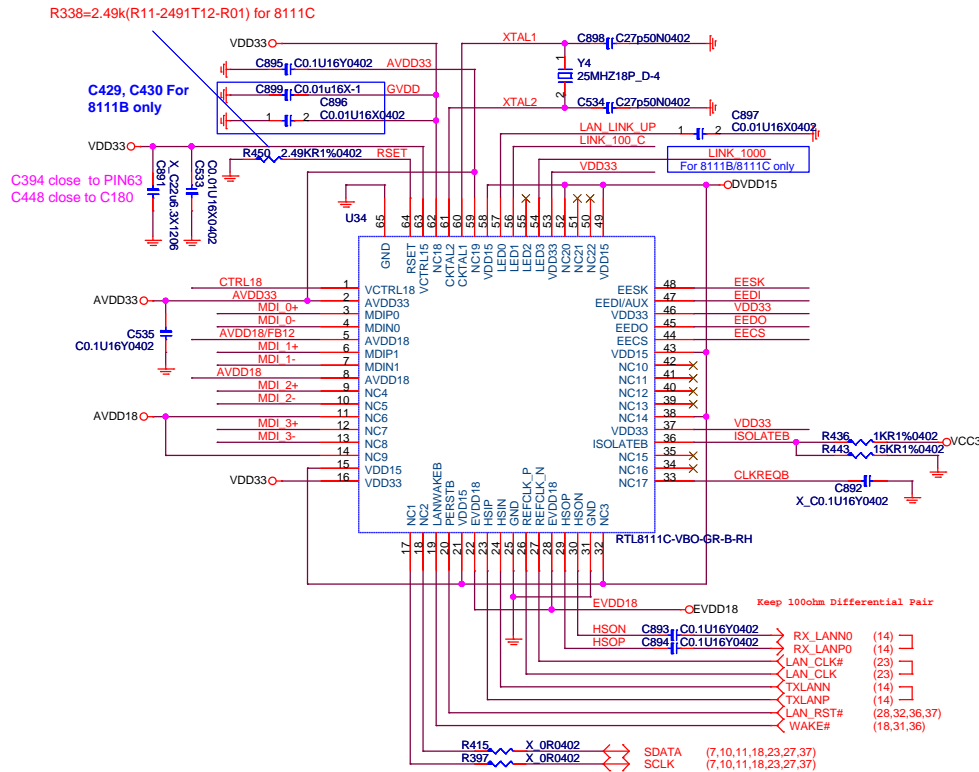
SERIAL ATA CONNECTOR BLOCK



PWM FAN CONTROL



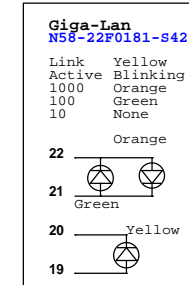
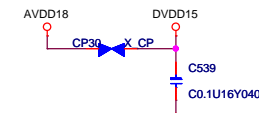
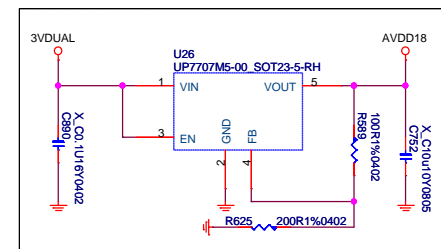
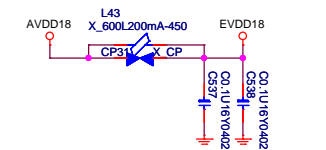
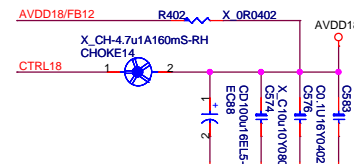
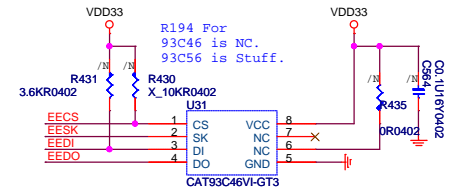
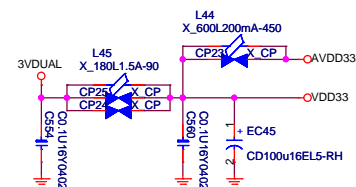
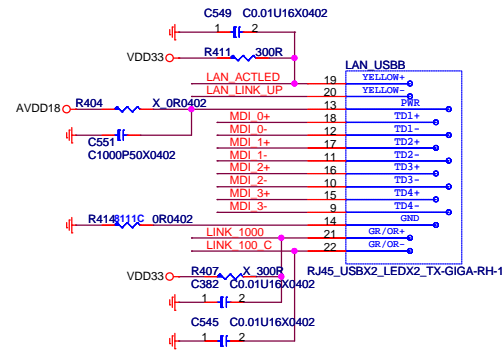
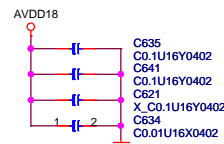
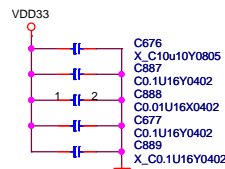
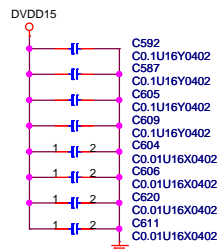
LAN - Realtek RTL8111C



Power domain chart

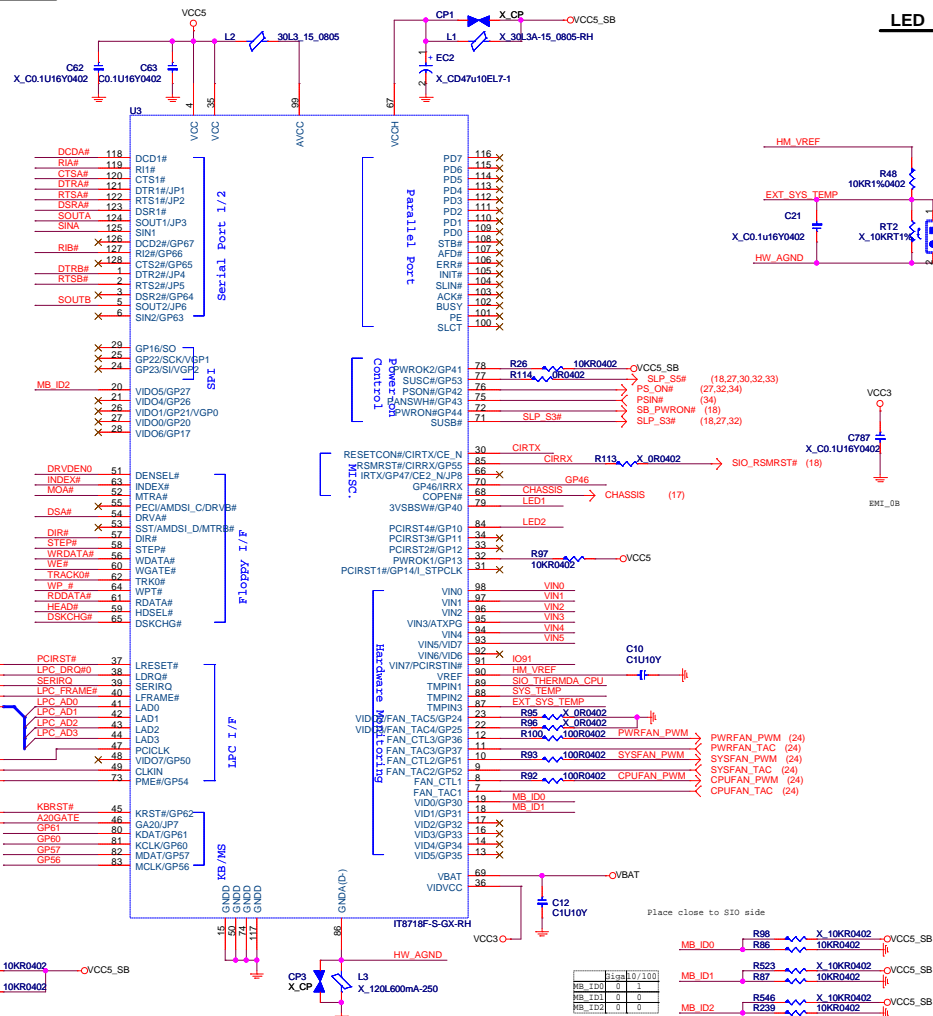
	RTL8111C
AVDD33	3.3V
AVDD18	1.2V
EVDD18	1.2V
DVDD15	1.2V

	8111C
VDD33	16,37,46,53
AVDD33	2,59
AVDD12	8,11,14,58
EVDD12	22,28
DVDD12	21,32,38,43,49,52
GND	65
AGND	25,31

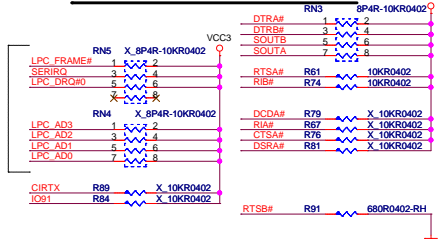


N58-22F0181-F02
N58-22F0181-S42

LPC I/O IT8718F



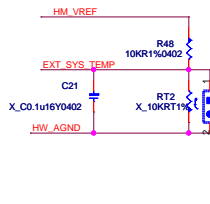
SUPER I/O STRAPPING RESISTOR



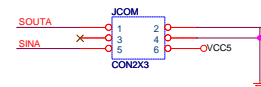
Power On Strapping Options

Symbol	value	Description
Flashseg1_EN	1	Disabled.
Flashseg1	0	Flash I/F Address Segment 1 (FFFF_0000h-FFFF_FFFFh, 000F_0000h-000F_FFFFh) is enabled
VIDO_SEL	1	Disable VIDOUT pins(except VIDO6 & VIDO7)
CHIP_SEL	0	Enable VIDOUT pins
BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# are open-drain.
FAN_CTL_SEL	0	The output buffers are push-pull.
VID_ISEL	1	The default value of EC Index 15h / 16h / 17h is 00h
	0	The default value of EC Index 15h / 16h / 17h is 40h
	1	The threshold voltage of VID is 2.0 / 0.8V
	0	The threshold voltage of VID is 0.8 / 0.4V

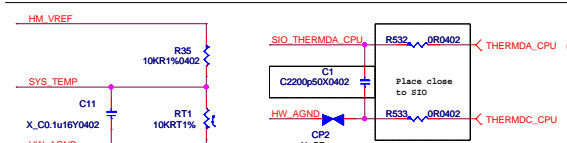
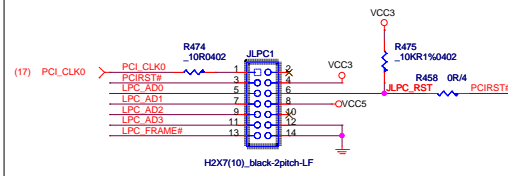
LED



SERIAL PORT 1



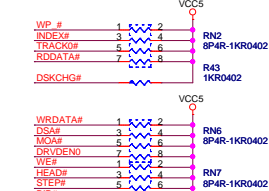
LPC DEBUG PORT



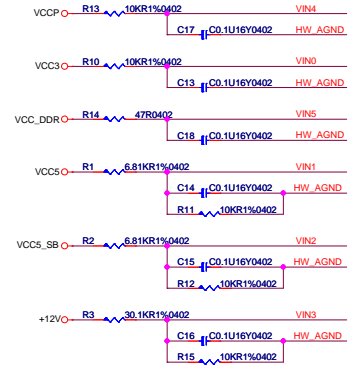
Super I/O Chassis



FLOPPY CONNECTOR



Thermal Resistor



SB700 & RS780 POWER GOOD CIRCUIT

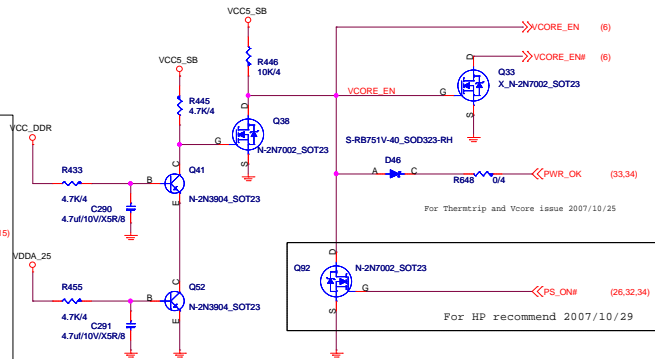
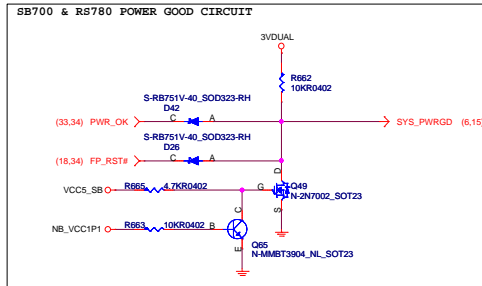


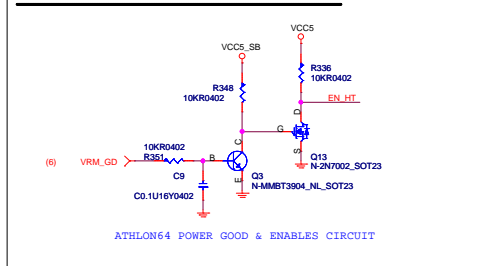
Table 15. Power Sequencing Group Definitions

Power Group A	Power Group B
VDDIO ^{1,2} <i>Vcc_DDR</i>	VDE[1:0] ³ <i>Vcore</i>
VTT ^{1,2} <i>VTT</i>	VDENB <i>Vcore_NB</i>
VDDA <i>VDDA33</i>	VLDI <i>HT</i>

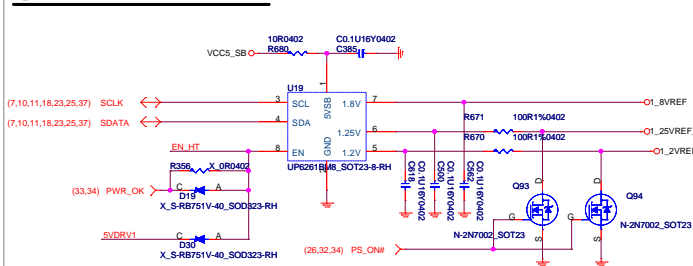
Notes:

- 1) *VDDIO must never exceed VTT by greater than X.XX V. This relationship must be enforced at all times including power-up, power-down, and power failure.*
- 2) *VDDIO and VTT only apply to DDR2 compatible processors.*
- 3) *VDD refers generically to the core voltage plane(s). VDD0 refers to processor power plane 0, and VDD1 refers to processor power plane 1.*

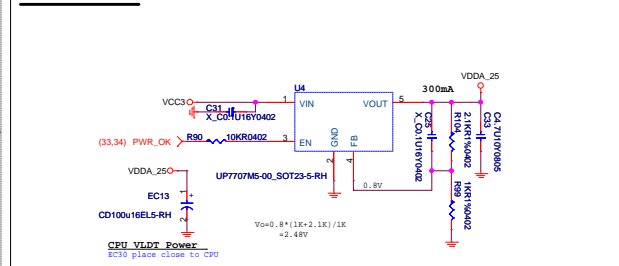
ATHLON64 POWER GOOD & ENABLES CIRCUIT



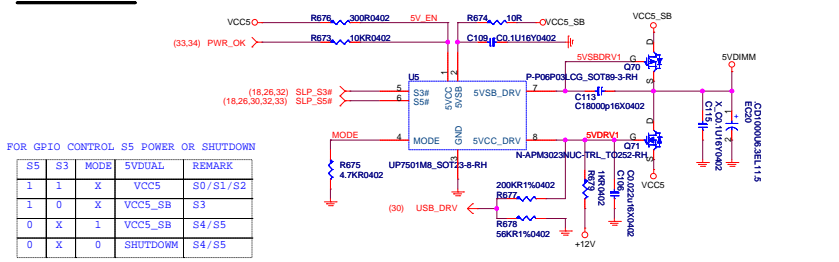
System Power Reference Source



VDDA_25 Power

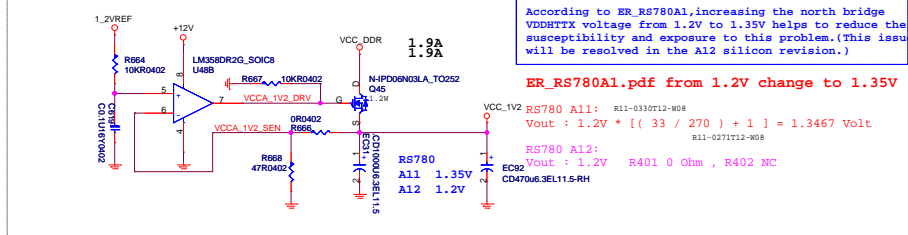


5V-DIMM Power

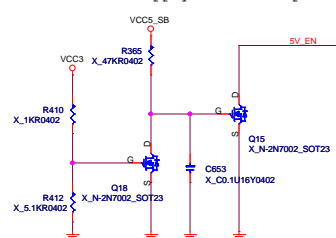


VCC_1V2 Power

For CPU, NB & +1.2V Power Rail
For SB VCC_SB +1.2V Power Rail

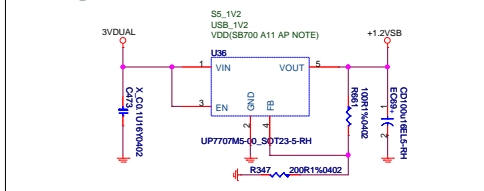


700W Power Supply for boot up issue

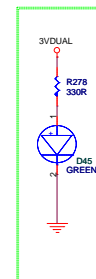


+1.2VSB
For SB +1.2V_SUS Power Rail

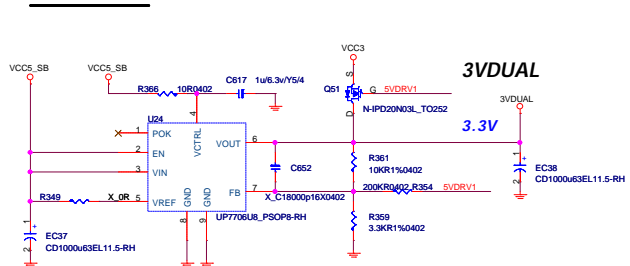
For SB +1.2V_SUS Power Rail



$$(V_{out} = 0.4 \times (R1 + R2) / R1 \text{ (V)})$$

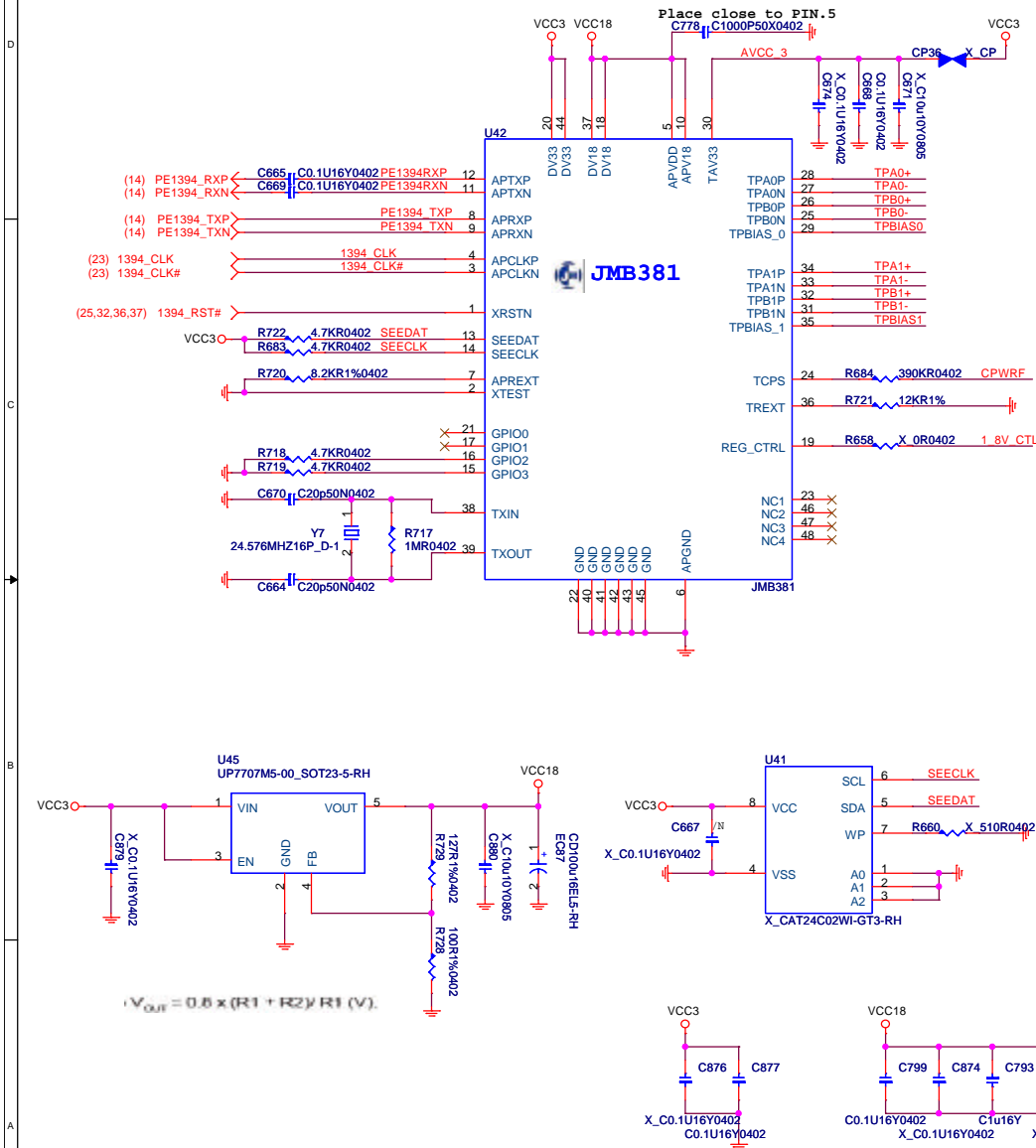


3VDUAL Power

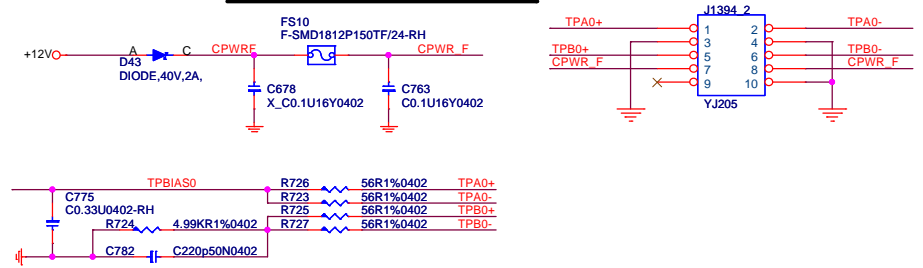


$$V_{OUT} = 0.8 \times (R1 + R2) / R2 \quad (V)$$

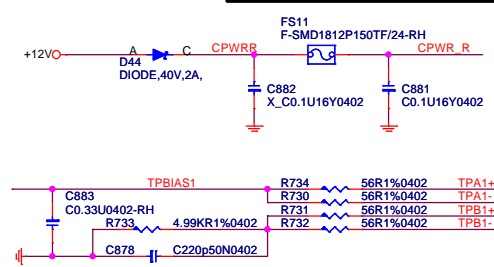
IEEE 1394 - JMicron JMB381



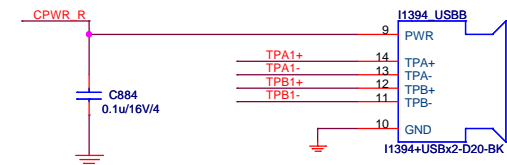
Front Side IEEE-1394 Port



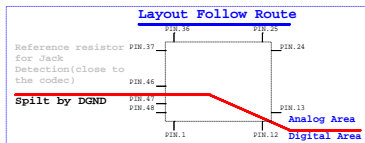
Rear Side IEEE-1394 Port



IEEE-1394 Port ESD



Default is ALC662

[illegible]

The schematic shows a 12V input connected to the LT1076 (U7) through a series combination of a resistor R901 (10K) and a capacitor C590 (100nF). The LT1076 is configured as a buck converter. The non-inverting input (pin 1) is connected to ground. The inverting input (pin 2) is connected to the output (pin 3) through a feedback network consisting of two resistors, R462 (100K) and R461 (334K), connected in series to ground. The output (pin 3) is connected to the load through a capacitor C615 (100nF). The LT1076 is also connected to a 1.8V reference (pin 4) and a 1.8V output (pin 5). The output is labeled A/D05. The diagram is divided into Digital Area and Analog Area sections.

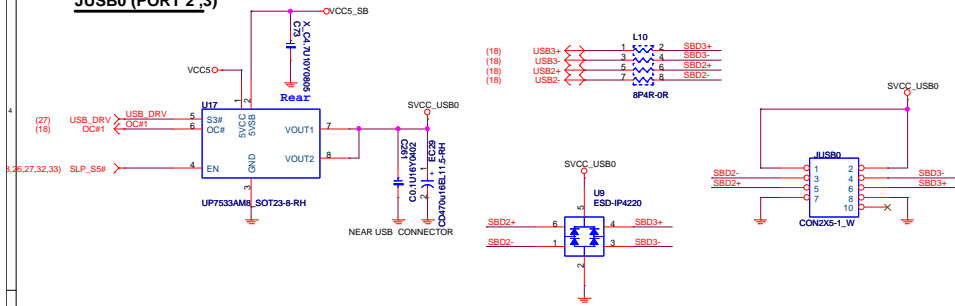
[illegible]

Figure 10 shows a 4-to-1 multiplexer circuit. The inputs are MIC_R, MIC_L, MP_R, and MP_L. The select lines are C673, C657, C663, and C660. The outputs are labeled X_C1000P60X0402. A legend indicates that MIC_R and MIC_L are connected to C673, MP_R to C657, and MP_L to C663. A note states "For SKI Placement close to Codec chip".

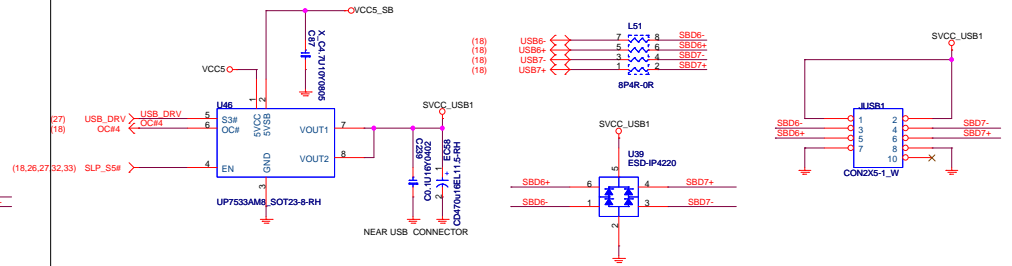
Schematic diagram of the SPIND_OUT signal path. The signal originates from the SPIND_OUT pin of the JAKO-RC43P module. It passes through a 100pF capacitor (C796) and a 221R150402 resistor (R513) to a 1004 resistor (R562). The signal then passes through a 0.01uF/50V capacitor (C821) to the G_SPIND_OUT pin of the JAKO-RC43P module.

Tied at one point only
under the codec or near
the codec

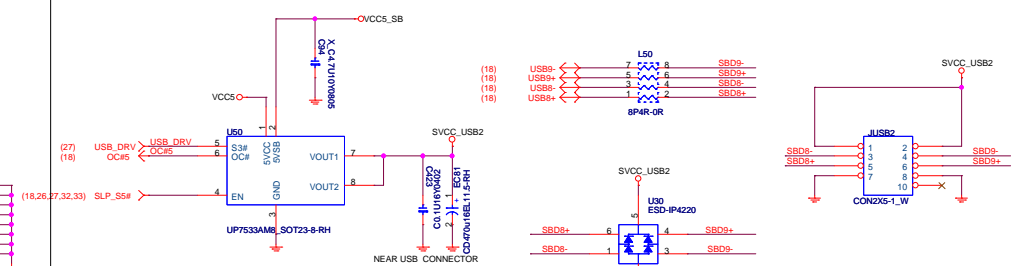
JUSB0 (PORT 2,3)



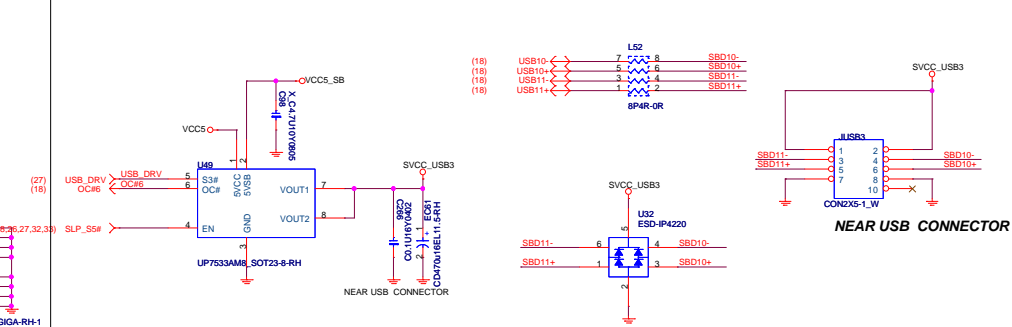
JUSB0 (PORT 6,7)



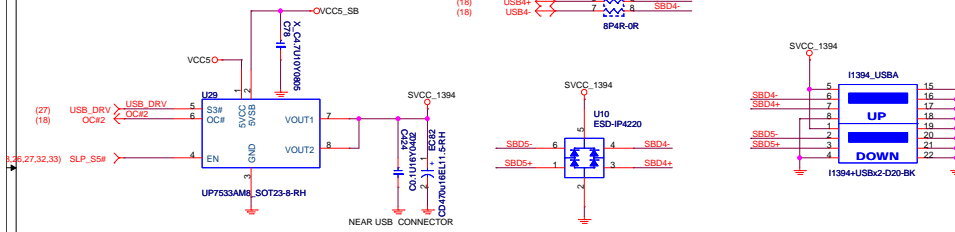
JUSB0 (PORT 8,9)



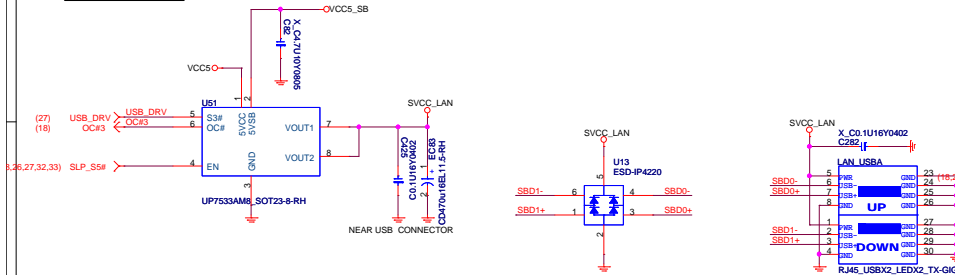
JUSB0 (PORT 10,11)



1394 USB PORT



LAN USB PORT

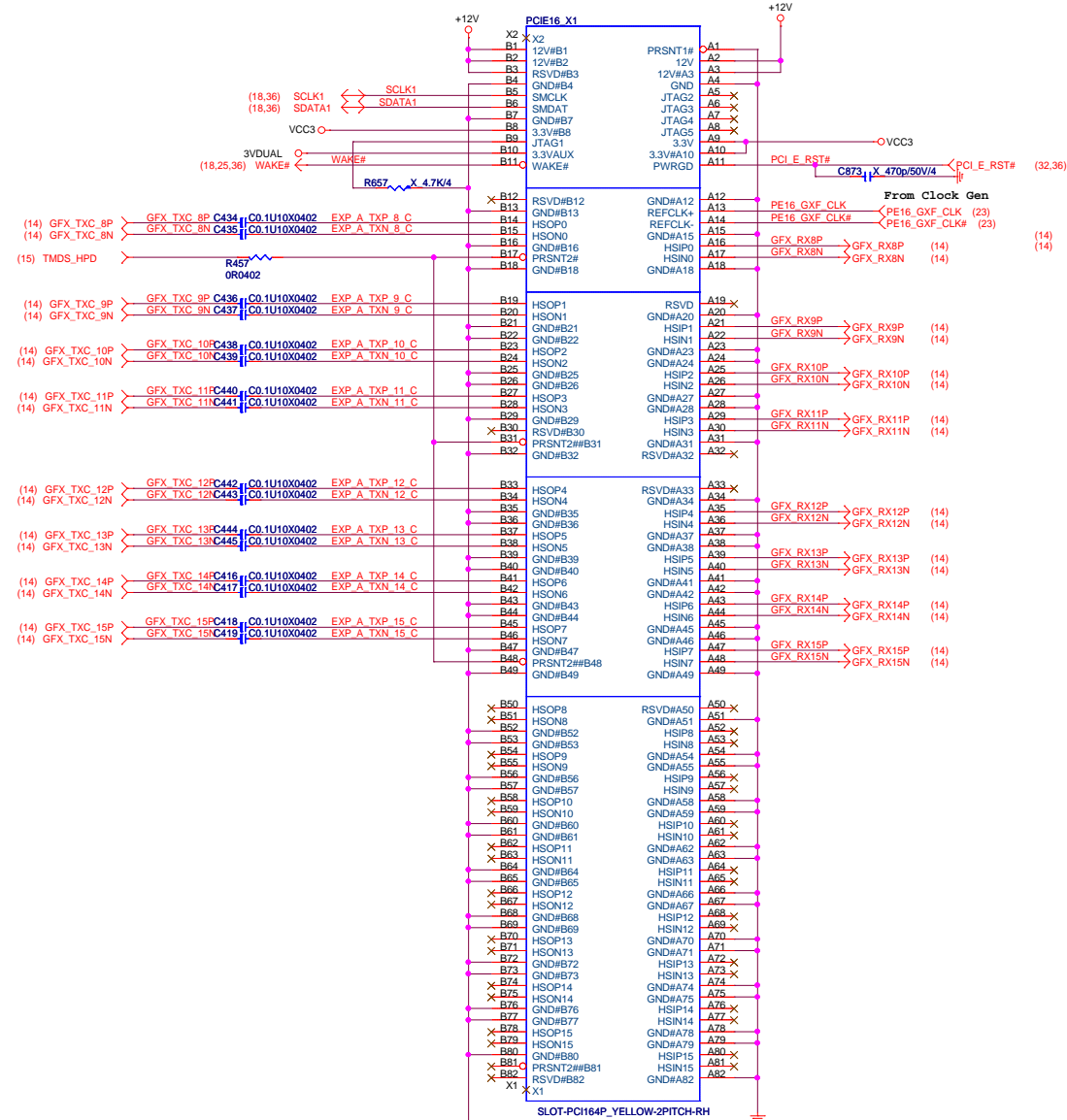


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

PCI Express Slot x16/x1

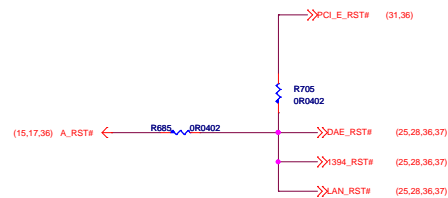
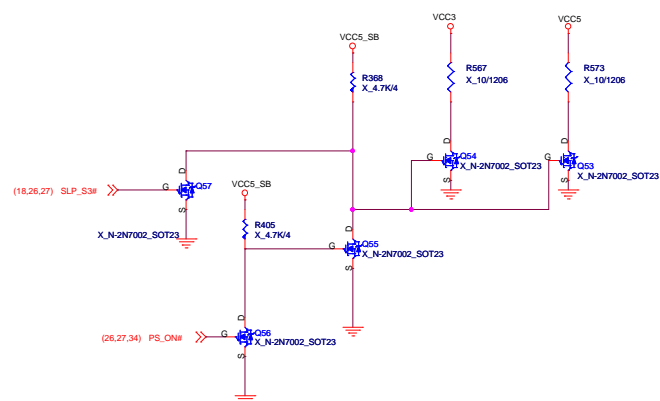
PCI EXPRESS x16 Slot



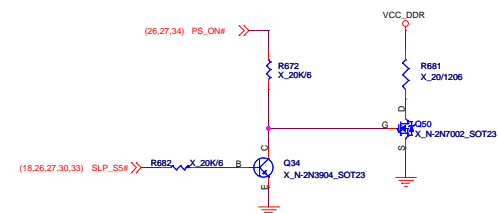
7.1.6 Residual Voltage Bleed-Off Circuit

A residual voltage circuit is required on the board. This circuit must be active in the S3, S4, and S5 state, whenever the main +5 V and +3.3 V power are turned off. A circuit diagram is shown below. When the system is in S3, S4, or S5, the transistors will be turned on, which will clamp any residual voltage on +5V and +3.3 V to ground. See the figure below for an example of a bleed-off circuit.

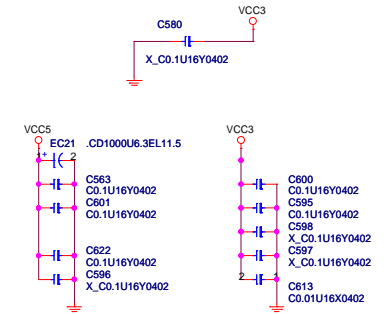
BLEED-OFF CIRCUIT



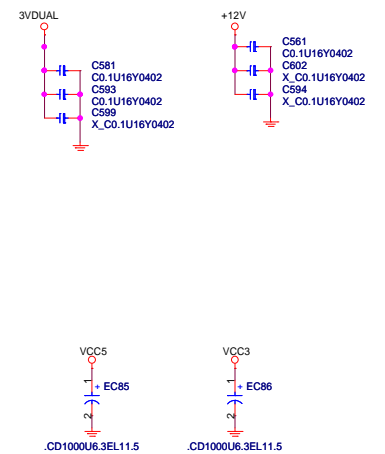
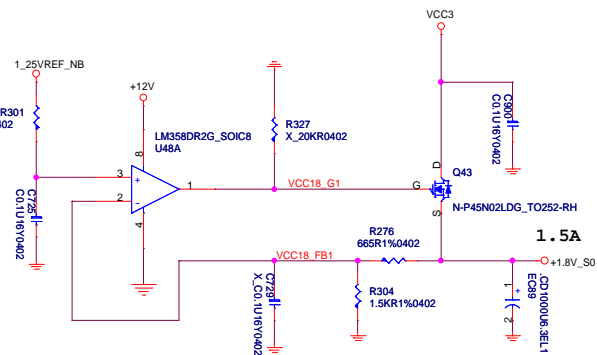
MEMORY VOLTAGE BLEED-OFF CIRCUIT



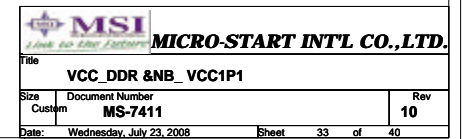
DDR II 1.8V POWER



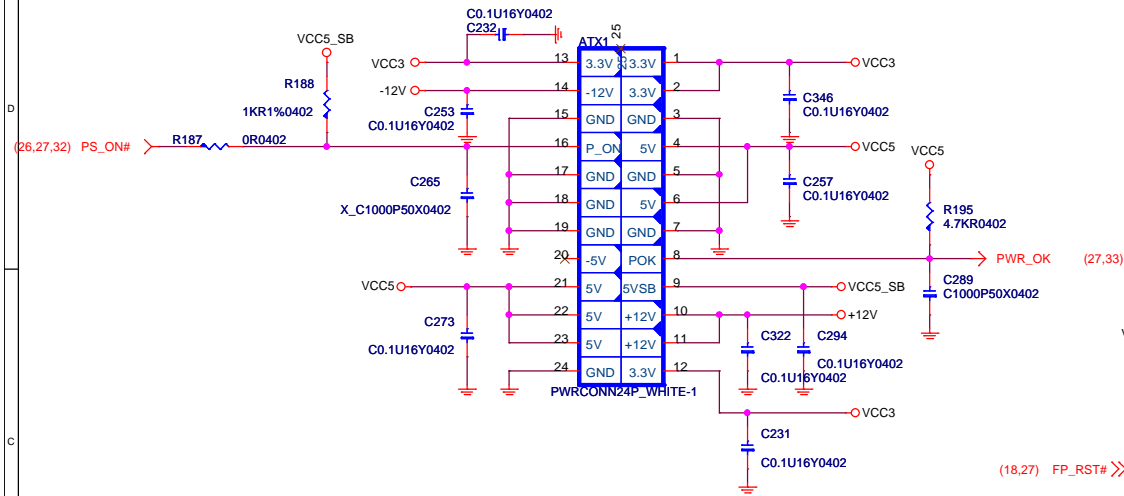
For NB +1.8V_S0 Power Rail



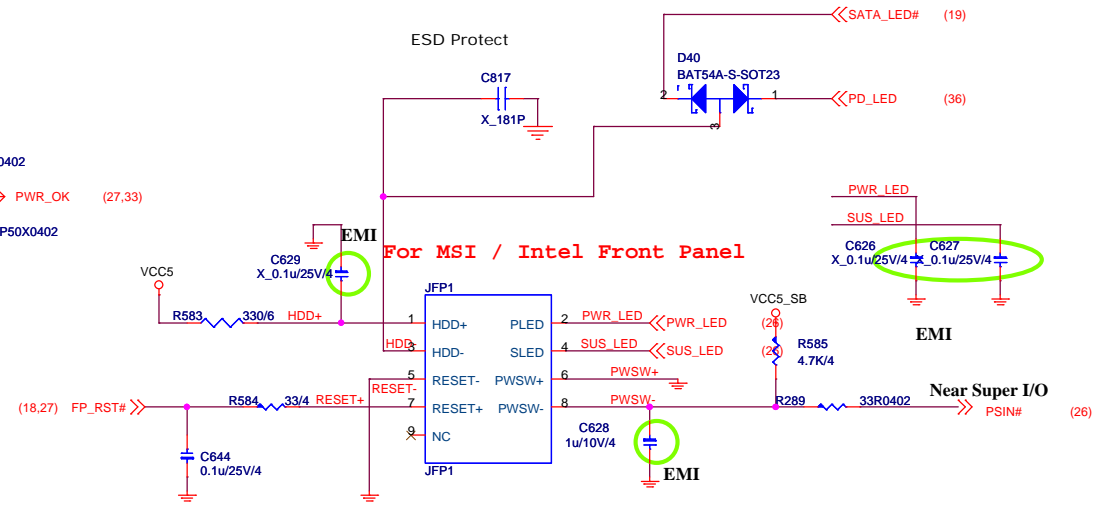
For NB +1.1V Power Rail



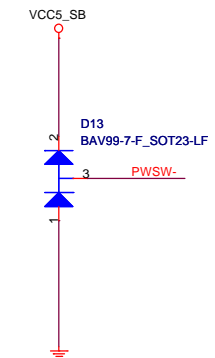
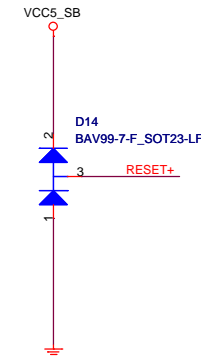
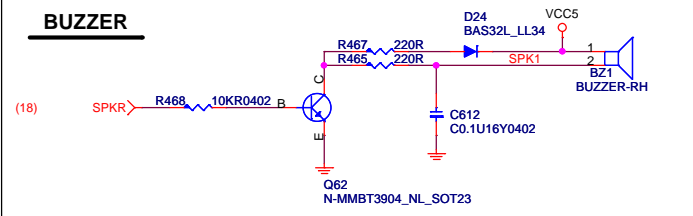
ATX CONNECTOR



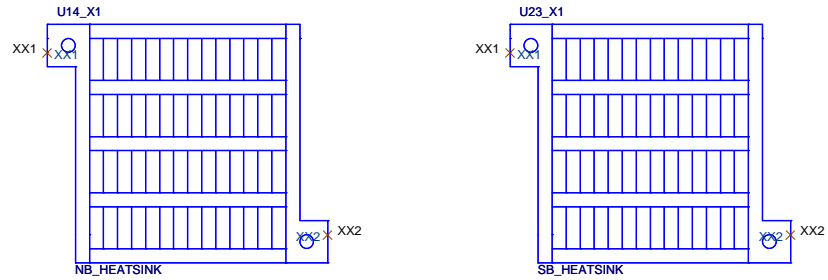
Intel Front Panel



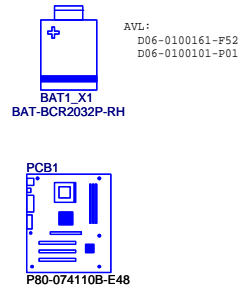
BUZZER



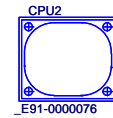
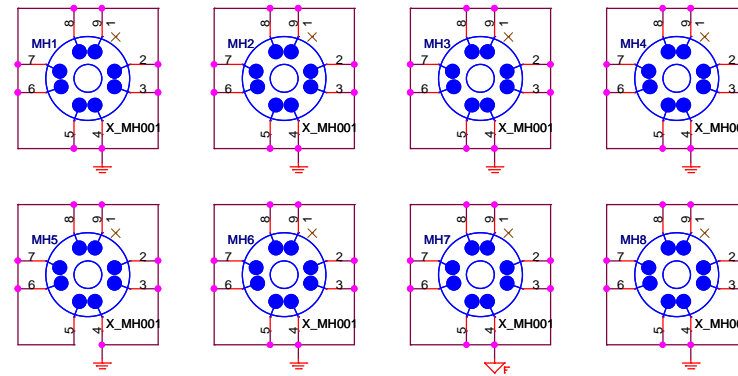
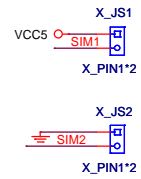
HEAT SINK



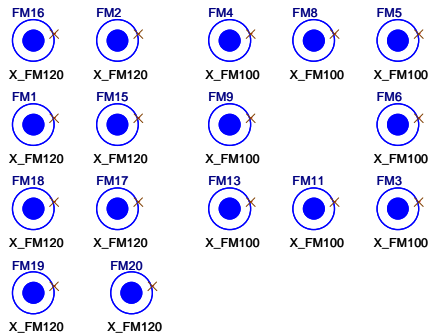
MANUAL PART




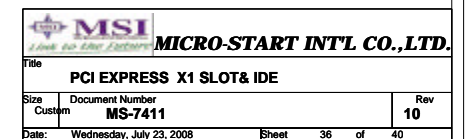
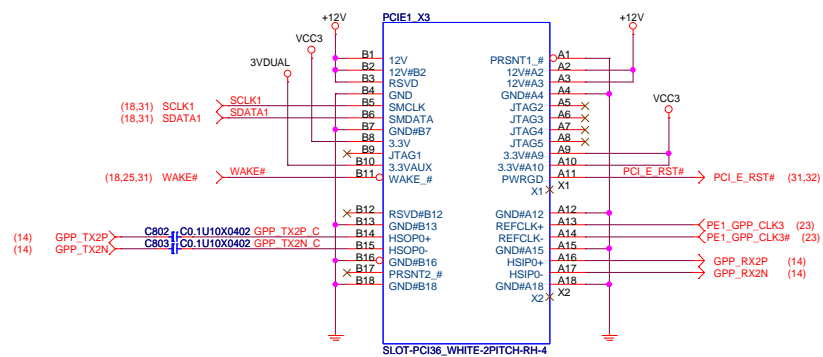
Simulation



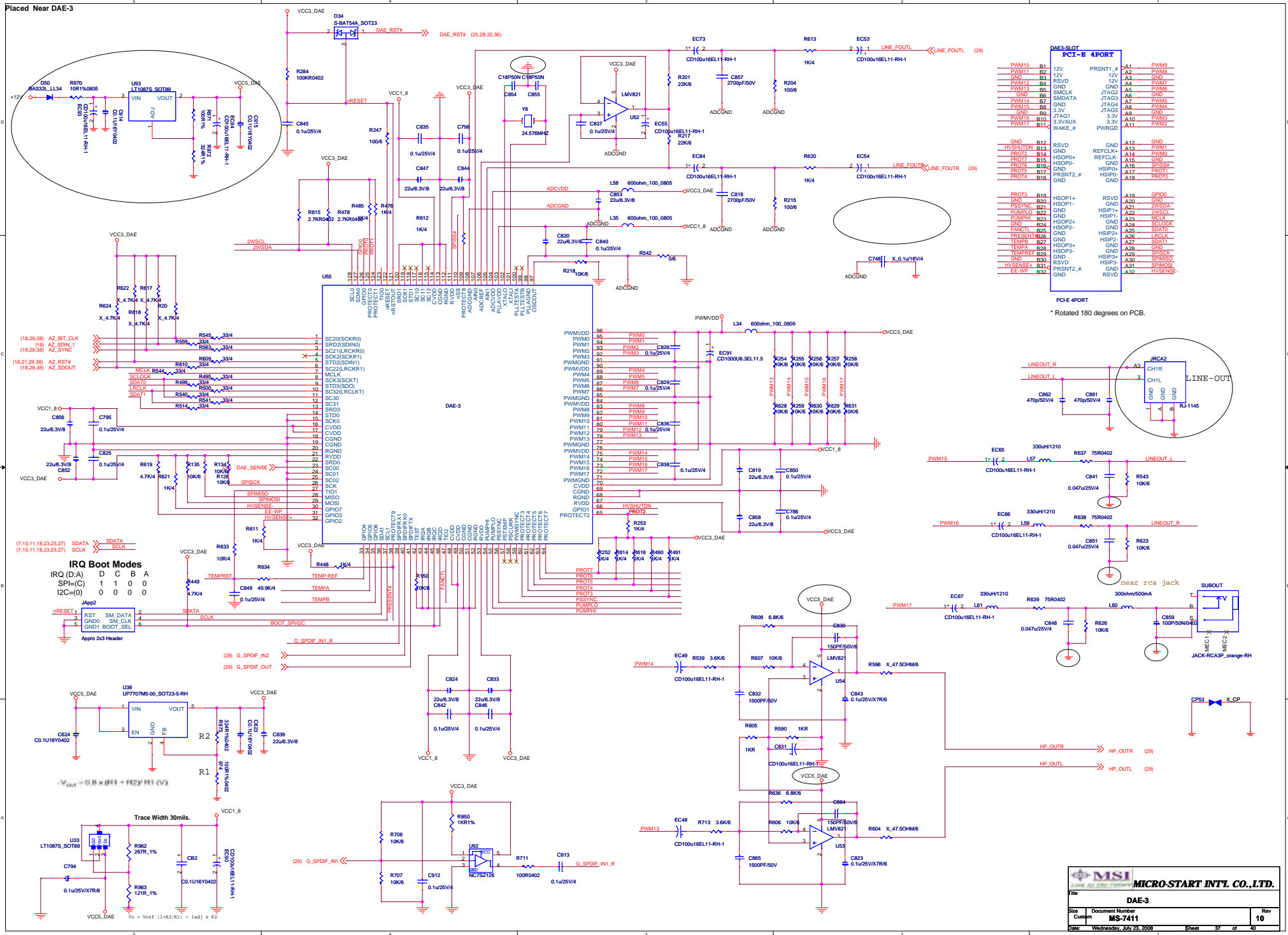
Optics Orientation Holes



 MICRO-START INTL CO.,LTD		
Title Auto BOM Mnaual		
Size B	Document Number MS-7411	Rev 10
Date: Wednesday, July 23, 2008	Sheet 35	of 40



Placed Near DAE-3



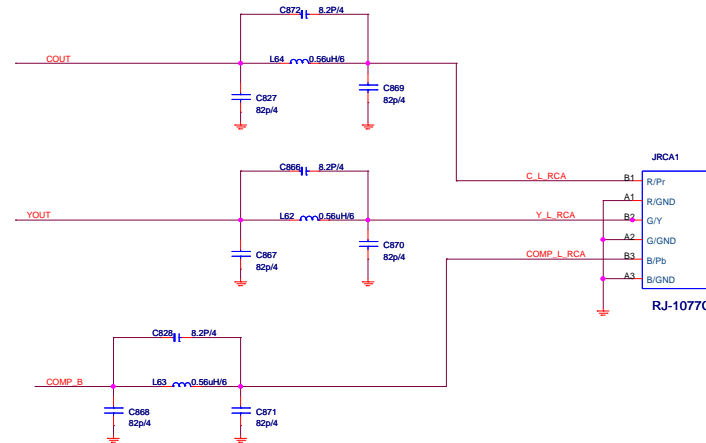
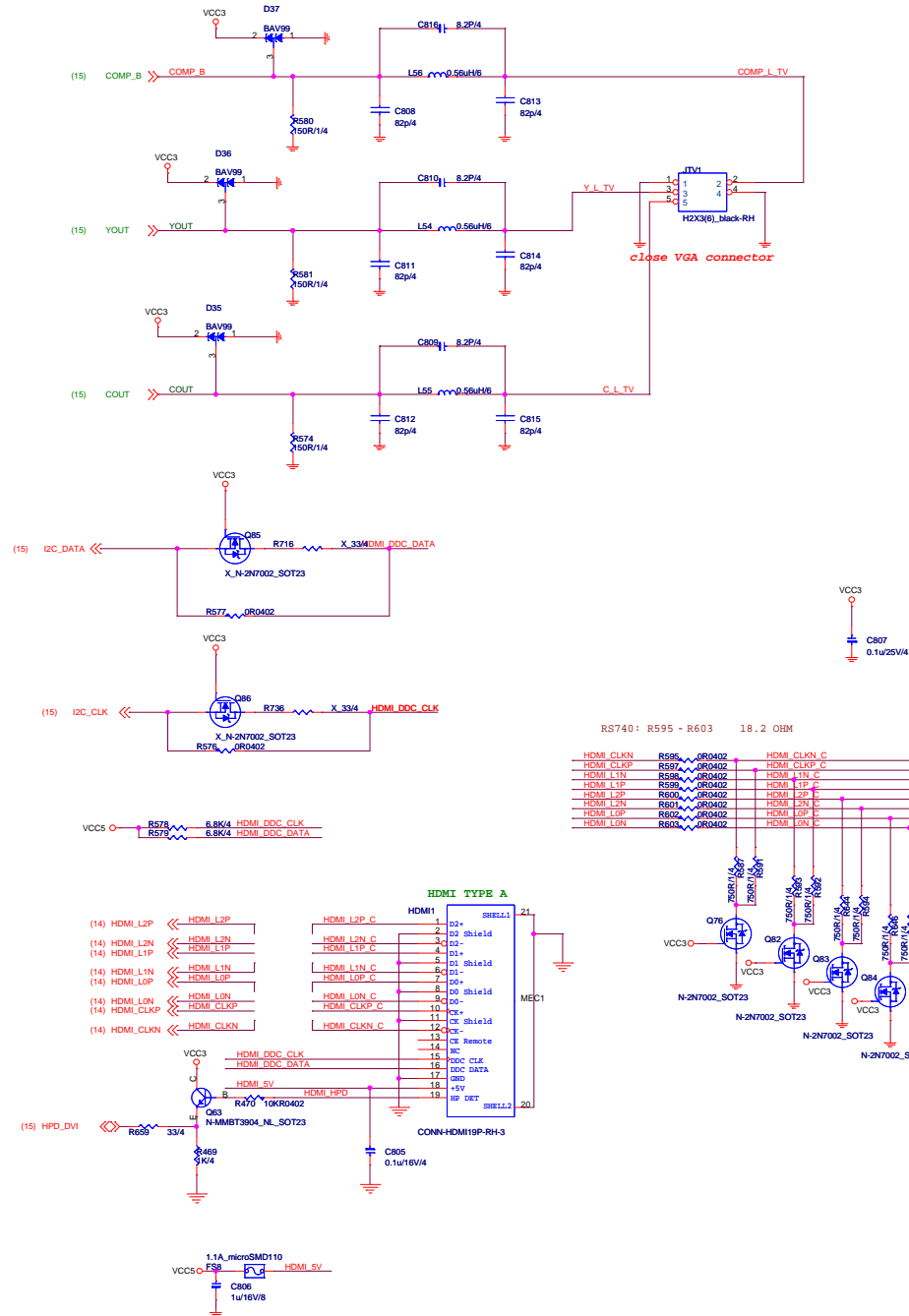
TV_OUT CONNECTOR

NOTE :reserve R188,R190,R193 2007/3/28

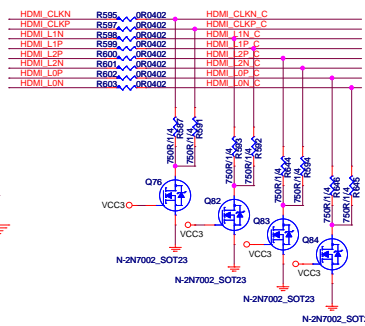
M6465 XPC Audio Connector



M6465 support VIDEO component out
2007/3/24



RS740: R595 - R603 18.2 OHM



Overall
Rev B to Rev 10
2008/04/11

Page01
Modify Cover Sheet

Page02
Modify System Block Diagram

Page03
Remove PCI Config Table

Page04
Modify clock distribution chart

Page05
Modify Power Deliver Chart

Page06
For Power Team Suggestion : VDD_NB,VCCP
1. R37 Change From 56K_1% ohm to 71.5K1%R0402 ohm (OCP)
2. R53 Change From 0 ohm to 200 ohm (ISEN_NB)
3. C48 Change From 0.01uF to 0.022 uF (Comp)
4. R62 Change From 3.4K_1% ohm to 6.98K_1% ohm (RC)
5. R120 Change From 1ohm to 0 ohm (U-Gate)
6. Choke 1 change From 0.25uH to 1.1uH
7. R31,R33,R65 Change From 200ohm to 300R1%0402

Page15
Added R965(Reserved for power sequence tuning)

Page29
Added R964 10K_1% to fix Line-In no Function issue

Page33
For Power Team Suggestion : VCC_DDR
1. Stuff R698 & Change From 41.2K_1% ohm to 26.1K_1% ohm (OCP)
2. CHOKE12 change to 1.1 uH
3. Stuff EC74 1000uF/6.3V

For Rev B Issue
1. R548.1 Connect to 1_25VREF_NB (Fixed net connect mistake)
2. R301.2 Connect to 1_25VREF_NB (Fixed net connect Mistake)
3. No Stuff C729 (Fixed +1.8V_S0 Power Noise)

Page36
R287 Added off-page connection (fixed net no connected issue)

Page37
No stuff R622 (Fixed Can't power on first time issue)

2008/04/16

Page15,38
Change R231 & R580 Value From 137 ohm to 150 ohm (Fixed BOM Mistake)

2008/04/24

For EMI Solution
(1) Added C549, C382, C545, C888, C604, C620, C606, C611, C634, C896, C897, C899(R0603), C755, C613, C648, C766, C765, C776, C754總共19顆電容C=10nF
(2) Added C779, C780總共2顆電容C=10pF

2008/04/28

Page26
Modify LED Circuit
1.Q47,Q48 Change to 2N7002
2.Added Q95,Q96 --> 2N7002
3.Added R966,R967 0 ohm 0402
4.Added R968,R969 0 ohm 0402 (No stuff)

Page22
Remove TPM Function (Component only)
No Stuff C631,C675,R313,R472,R582,R641,U56,Y9

2008/05/12

Page29
1.Delete JRCA2
2.R462 change to 100 ohm 1%(0603),R461 Change to 324 ohm 1%(0603)
3.Added JRCA3
4.C658 位置需調整(Layout)

Page28
1.U45 change to uP 7707, R127 change to 127 ohm 1%(0402)

Page37
1.U53.5,U54.5 Connect to VCC5_DAE
2.C841.2, R543.1, C851.2, R623.1, C848.2, R626.1, C859.1 , SUBOUT.S, Connect to GND
3.ADCGND rename to GNDF (Analog Ground)
4.C854.1, C855.2 Connect to GND
5.ADDED JRCA2
6.Added D50,R970,R971,R972,EC93,EC94,C914,C915,U93
7.U38 change to uP 7707, EC90 change to 100uF
8.Added R973,R974,EC91

Page31
1.Stuff R457 0 ohm

Page32
1.Delete U102

Page24
1.R464,R466,R479,R480,R481,R494,R496,R551 CHANGE TO 0 ohm(for sata SI issue)
2.Rename SATA connector (silkscreen only)

Page23
1.No stuff R271,R272,R273,R275

Page27
1.STUFF R668 47 ohm 1% 0402

Page33
1.EC89 change to 1000uF

Page29
1.R461 change to 324 ohm 1%
2.R462 change to 100 ohm 1%

2008/05/14

Page33
1.Remove EC75 , EC76

Page13
1.U21 Change to M12-K4N1G15-S02

Page37
1.U55 Change footprint to LQFP128_0_4MM

2008/05/15

Page37
1.JRCA2 Change to ON5-7411007


Page29
1.JRCA3 Change to ON5-7411007
2.Add R974,R975

2008/05/16

1. Q14, Q20, Q23, Q6, Q79, Q44 change to D03-09N030B-I14
2. Q16, Q17, Q21, Q22, Q28, Q27, Q7, Q8, Q80, Q46 change to D03-06N030B-I14

2008/05/19

1.Delete EC57,EC68
2.EC3,EC33,EC41,C831,EC48,EC49,EC90,EC93,EC55,EC65,EC66,EC67,EC53,EC54,EC73,EC84 CHANGE TO C93-1011611-P01
3.EC46,EC47 CHANGE TO C93-1011621-T30
4.Delete C658


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BOM Change List

Rev.B to Rev.10

Rev.10 to Rev.11

- 1.Add CP53
- 2.remove FM7
- 3.E15 change to R51-0103T91-T43
- 4.FS10,FS11 change to D08-0200230-P16

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Title Revision History-2		
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